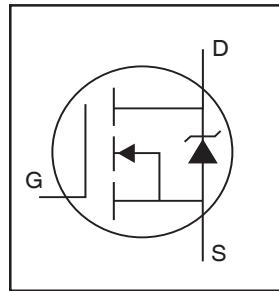


HEXFET® Power MOSFET

Features

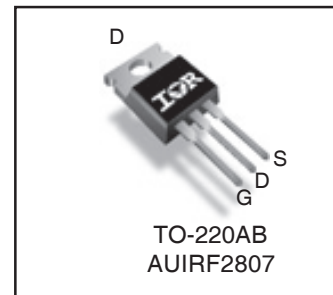
- Advanced Planar Technology
- Low On-Resistance
- Dynamic dV/dT Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *



$V_{(BR)DSS}$	75V
$R_{DS(on)}$ max.	13mΩ
I_D (Silicon Limited)	82A Ⓢ
I_D (Package Limited)	75A

Description

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	82Ⓢ	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	58	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	75	
I_{DM}	Pulsed Drain Current ①	280	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	230	W
	Linear Derating Factor	1.5	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②③	340	mJ
I_{AR}	Avalanche Current ①	43	A
E_{AR}	Repetitive Avalanche Energy ①	23	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.9	V/ns
T_J	Operating Junction and Storage Temperature Range	-55 to + 175	°C
T_{STG}			
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.65	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

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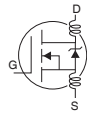
*Qualification standards can be found at <http://www.irf.com/>

Static Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	75	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.074	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	13	mΩ	V _{GS} = 10V, I _D = 43A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	38	—	—	S	V _{DS} = 50V, I _D = 43A ④
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 75V, V _{GS} = 0V
		—	—	250		V _{DS} = 60V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V

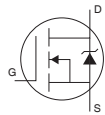
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Q _g	Total Gate Charge	—	—	160	nC	I _D = 43A V _{DS} = 60V V _{GS} = 10V, See Fig.6 and 13 ④
Q _{gs}	Gate-to-Source Charge	—	—	29		
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	55		
t _{d(on)}	Turn-On Delay Time	—	13	—	ns	V _{DD} = 38V I _D = 43A R _G = 2.5Ω V _{GS} = 10V, See Fig.10 ④
t _r	Rise Time	—	64	—		
t _{d(off)}	Turn-Off Delay Time	—	49	—		
t _f	Fall Time	—	48	—		
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) Between lead, and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	3820	—	pF	V _{GS} = 0V V _{DS} = 25V f = 1.0MHz, See Fig.5
C _{oss}	Output Capacitance	—	610	—		
C _{rss}	Reverse Transfer Capacitance	—	130	—		



Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	82 ⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	280		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 43A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	100	150	ns	T _J = 25°C, I _F = 43A
Q _{rr}	Reverse Recovery Charge	—	410	610	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T_J = 25°C, L = 370μH, R_G = 25Ω, I_{AS} = 43A, V_{GS} = 10V (See Figure 12)
- ③ I_{SD} ≤ 43A, di/dt ≤ 300A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ This is a calculated value limited to T_J = 175°C .
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

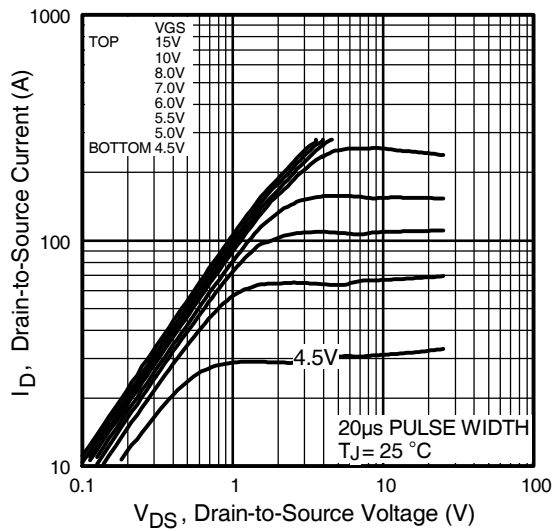


Fig 1. Typical Output Characteristics

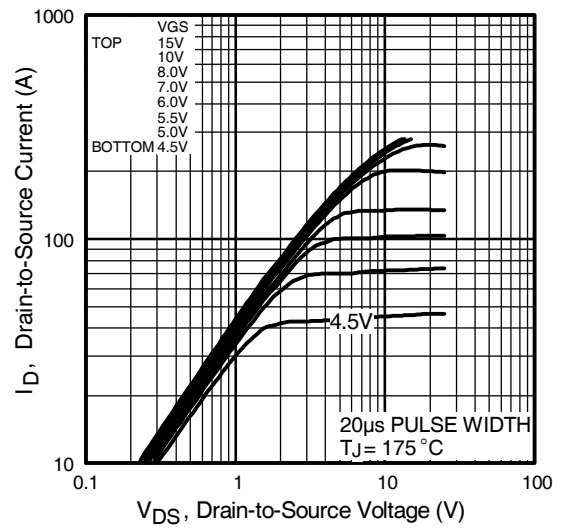


Fig 2. Typical Output Characteristics

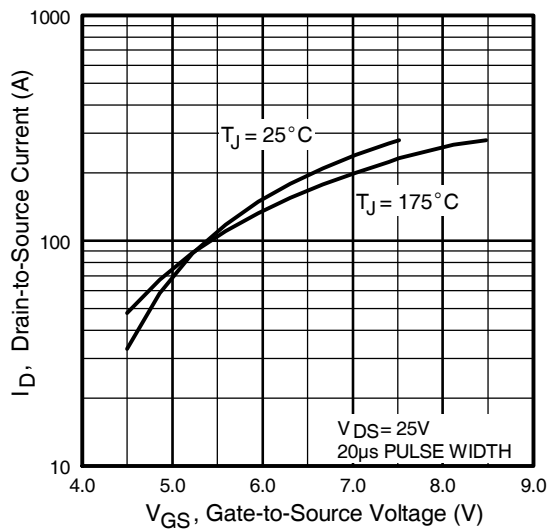


Fig 3. Typical Transfer Characteristics

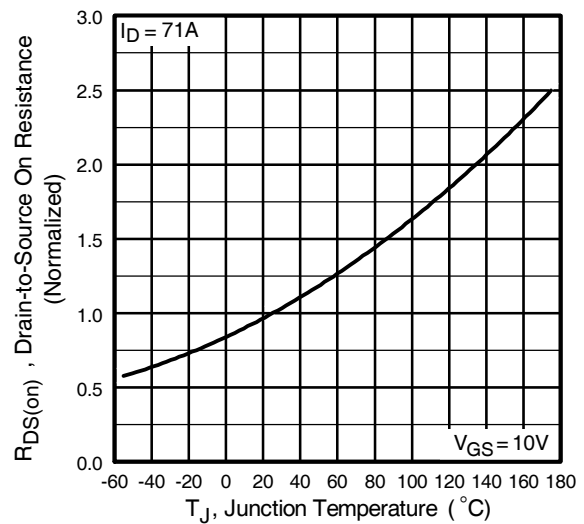


Fig 4. Normalized On-Resistance Vs. Temperature

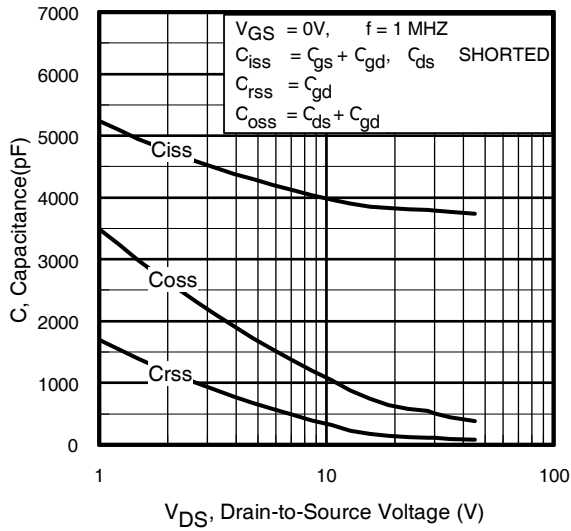


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

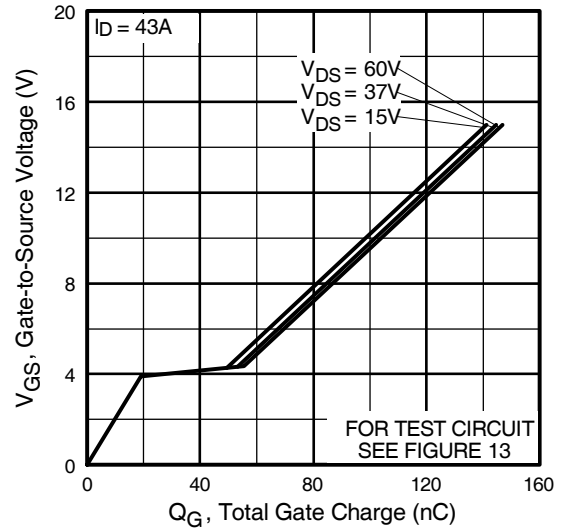


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

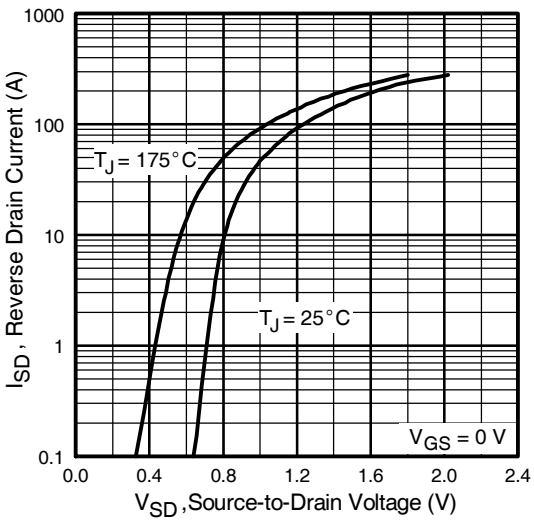


Fig 7. Typical Source-Drain Diode Forward Voltage

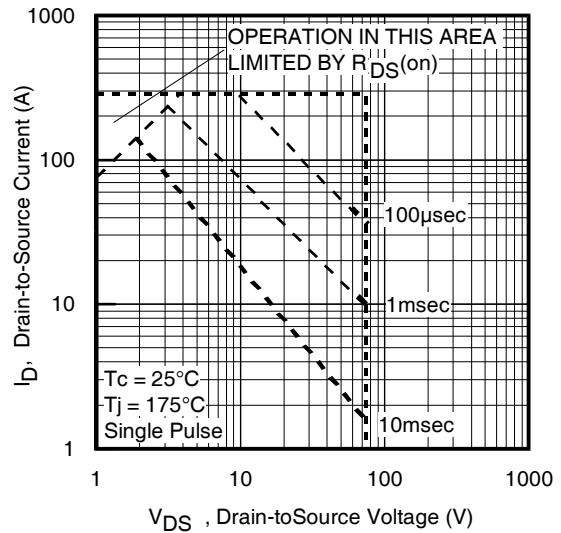


Fig 8. Maximum Safe Operating Area

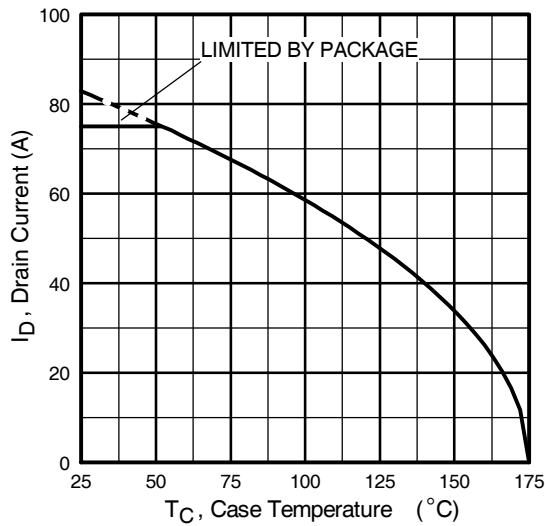


Fig 9. Maximum Drain Current Vs. Case Temperature

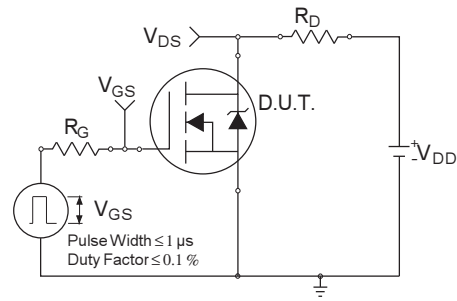


Fig 10a. Switching Time Test Circuit

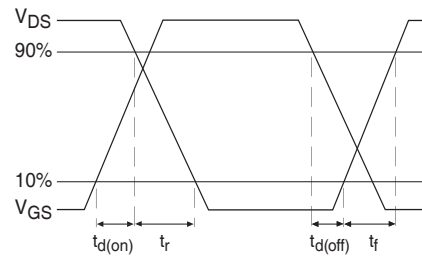


Fig 10b. Switching Time Waveforms

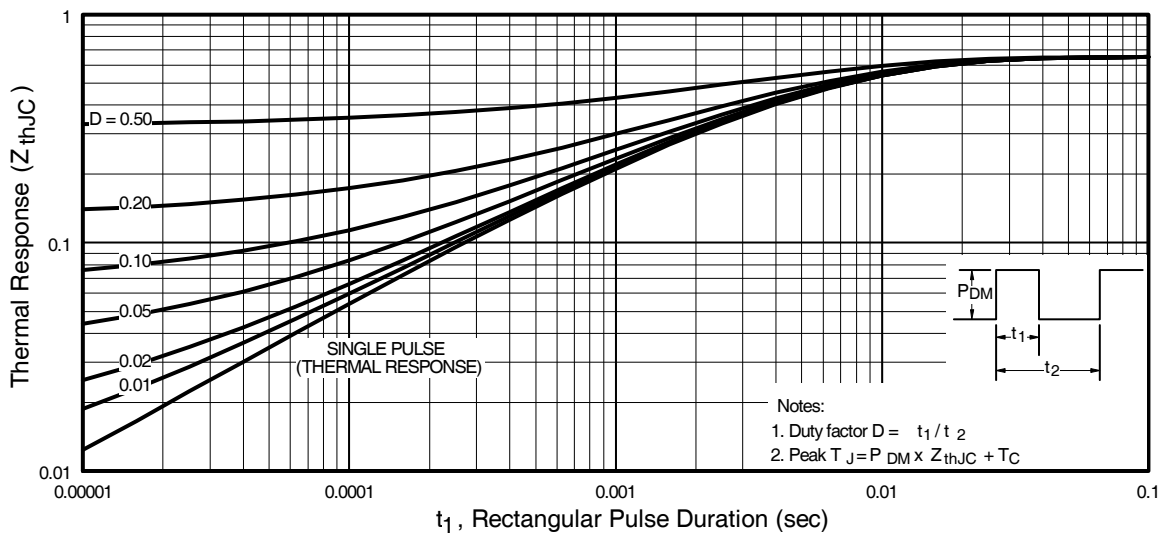


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

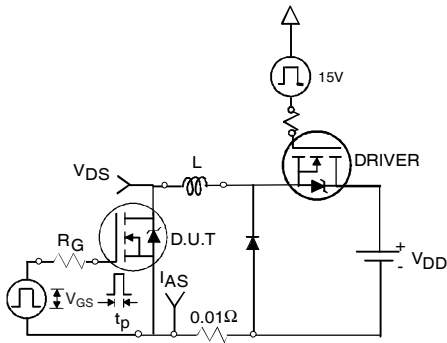


Fig 12a. Unclamped Inductive Test Circuit

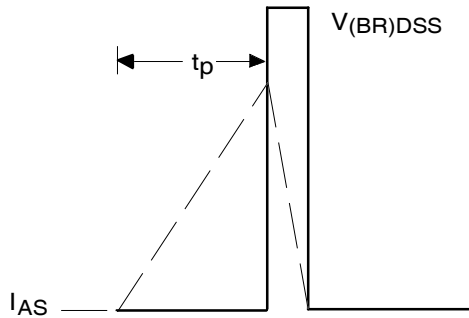


Fig 12b. Unclamped Inductive Waveforms

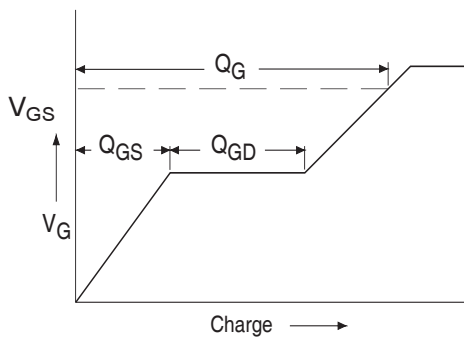


Fig 13a. Basic Gate Charge Waveform

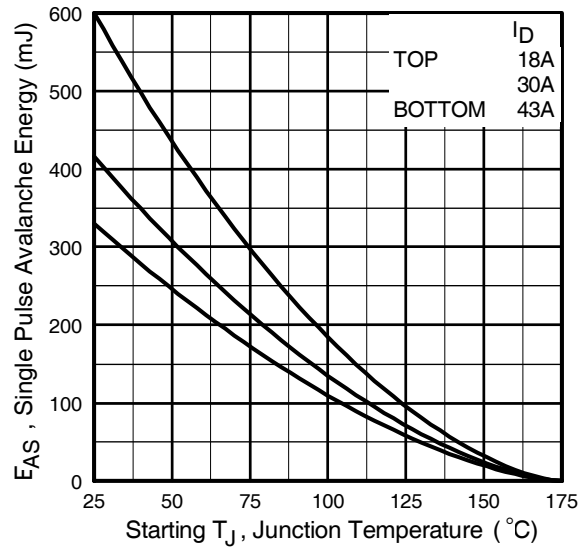


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

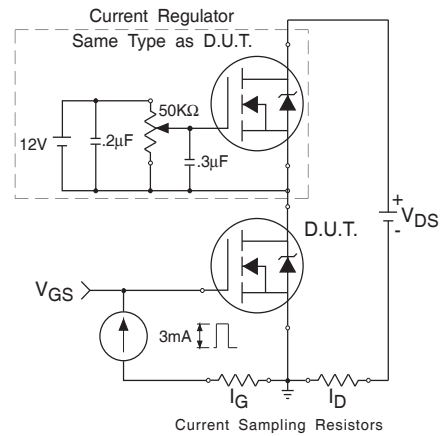
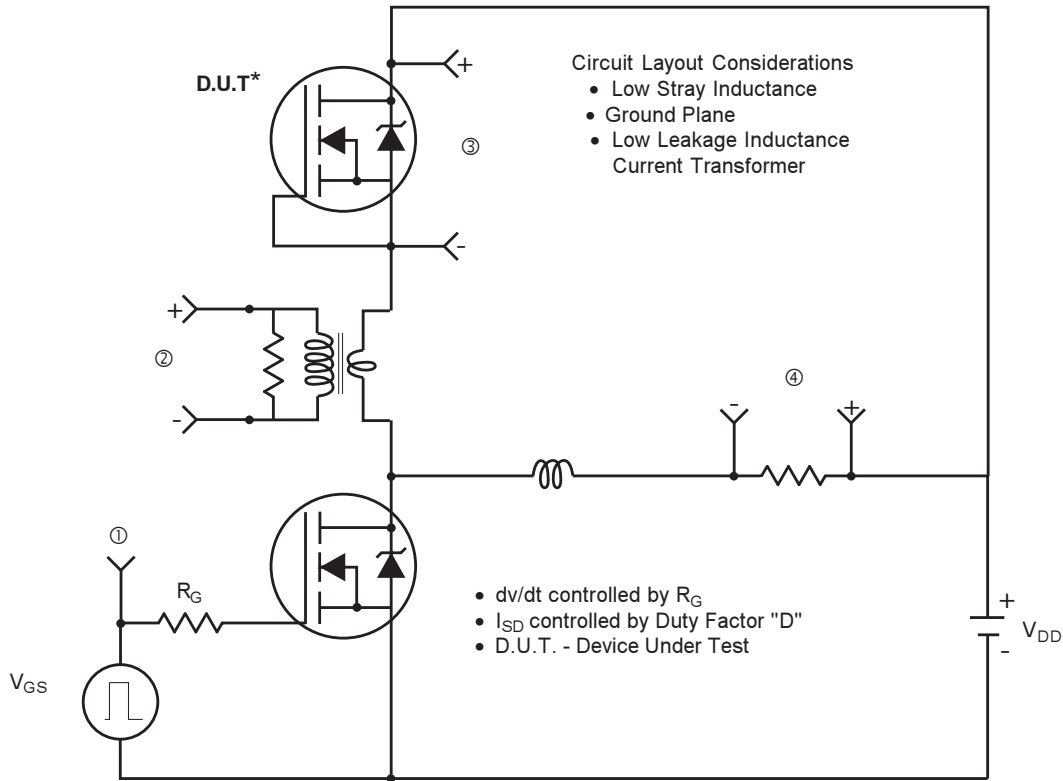


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel

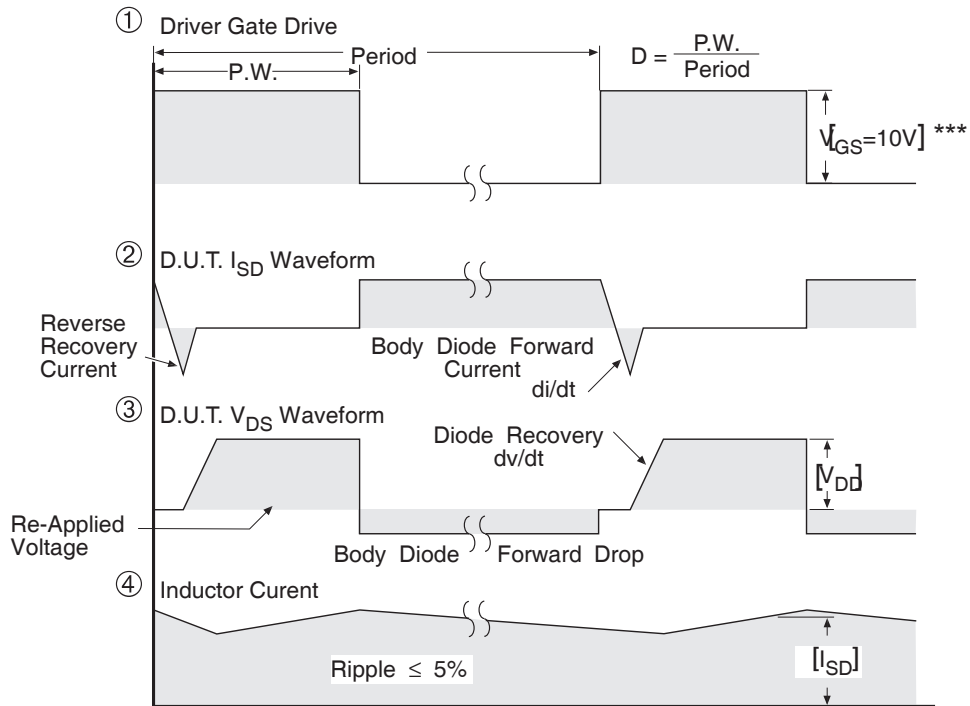
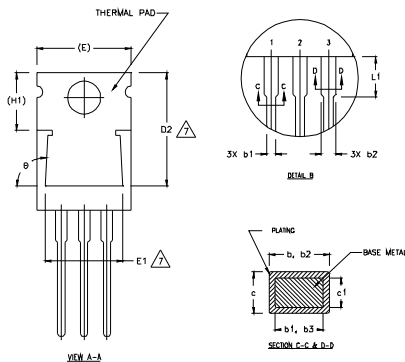
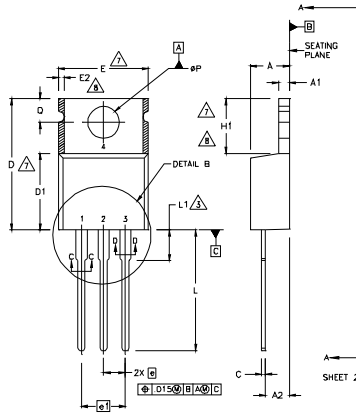


Fig 14. For N-channel HEXFET® power MOSFETs

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5 DIMENSION b1 & c1 APPLY TO BASE METAL ONLY.
- 6 CONTROLLING DIMENSION : INCHES.
- 7 THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8 DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.

LEAD ASSIGNMENTS

HEXFEET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs - CoPACK

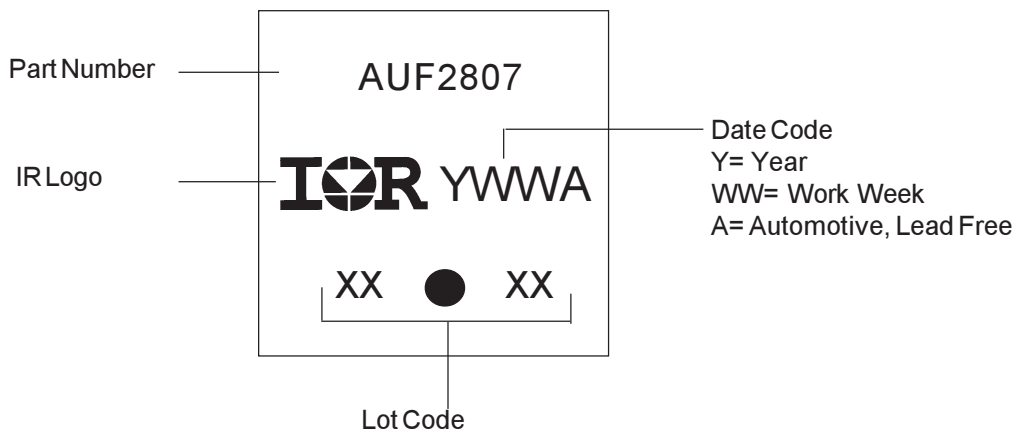
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

DIODES

- 1 - ANODE/OPEN
- 2 - CATHODE
- 3 - ANODE

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.82	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.04	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.96	.015	.038	5
b2	1.15	1.77	.045	.070	
b3	1.15	1.73	.045	.068	
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	12.19	12.88	.480	.507	7
E	9.66	10.66	.380	.420	4,7
E1	8.38	8.89	.330	.350	7
e	2.54 BSC		.100 BSC		
e1	5.08		.200 BSC		
H1	5.85	6.55	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	-	6.35	-	.250	3
ØP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	
φ	90°-93°		90°-93°		

TO-220AB Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Ordering Information

Base part	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRF2807	TO-220	Tube	50	AUIRF2807

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Tel: (310) 252-7105