International
IOR Rectifier

AUTOMOTIVE GRADE

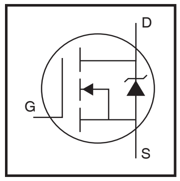
PD - 97698

AUIRF3808S

HEXFET® Power MOSFET

Features

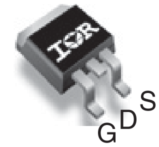
- Advanced Planar Technology
- Low On-Resistance
- Dynamic dV/dT Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *



V_{DSS}		**75V**
$R_{DS(on)}$	typ.	**5.9mΩ**
	max.	**7.0mΩ**
I_D		**106A**

Description

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.



D^2Pak
AUIRF3808S

G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, VGS @ 10V	106	A
I_D @ T_C = 100°C	Continuous Drain Current, VGS @ 10V	75	
I_{DM}	Pulsed Drain Current ①	550	
P_D @T_C = 25°C	Maximum Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	430	mJ
I_{AR}	Avalanche Current ①	82	A
E_{AR}	Repetitive Avalanche Energy ①	See Fig. 12a, 12b, 15, 16	mJ
dv/dt	Peak Diode Recovery ③	5.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	——	0.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state) ⑦	——	40	

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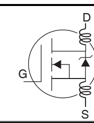
*Qualification standards can be found at http://www.irf.com/

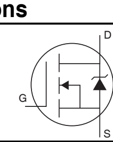
Static Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.086	——	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	5.9	7.0	mΩ	V_{GS} = 10V, I_D = 82A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
gfs	Forward Transconductance	100	——	——	S	V_{DS} = 25V, I_D = 82A
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	μA	V_{DS} = 75V, V_{GS} = 0V
		——	——	250		V_{DS} = 60V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	——	150	220	nC	I_D = 82A
Q_{gs}	Gate-to-Source Charge	——	31	47		V_{DS} = 60V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	50	76		V_{GS} = 10V ④
$t_{d(on)}$	Turn-On Delay Time	——	16	——	ns	V_{DD} = 38V
t_r	Rise Time	——	140	——		I_D = 82A
$t_{d(off)}$	Turn-Off Delay Time	——	68	——		R_G = 2.5Ω
t_f	Fall Time	——	120	——		V_{GS} = 10V ④
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.)
L_S	Internal Source Inductance	——	7.5	——		from package and center of die contact 
C_{iss}	Input Capacitance	——	5310	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	890	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	130	——		ƒ = 1.0 MHz, See Fig. 5
C_{oss}	Output Capacitance	——	6010	——		V_{GS} = 0V, V_{DS} = 1.0V, ƒ = 1.0MHz
C_{oss}	Output Capacitance	——	570	——		V_{GS} = 0V, V_{DS} = 60V, ƒ = 1.0MHz
C_{oss} eff.	Effective Output Capacitance (Time Related)	——	1140	——		V_{GS} = 0V, V_{DS} = 0V to 60V

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	106	A	MOSFET symbol showing the
I_{SM}	Pulsed Source Current (Body Diode) ②	——	——	550	A	integral reverse p-n junction diode. 
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 82A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	93	140	ns	T_J = 25°C, I_F = 82A
Q_{rr}	Reverse Recovery Charge	——	340	510	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Starting T_J = 25°C, L = 0.130mH R_G = 25Ω, I_{AS} = 82A. (See Figure 12).

③ $I_{SD} \leq$ 82A, di/dt ≤ 310A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C

④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑧ R_θ is measured at T_J approximately 90°C.

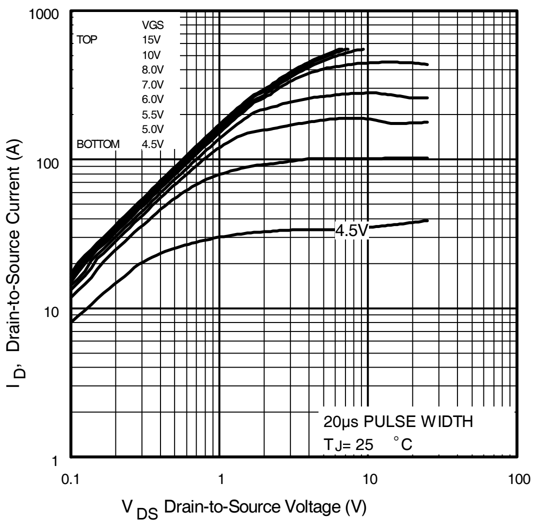


Fig 1. Typical Output Characteristics

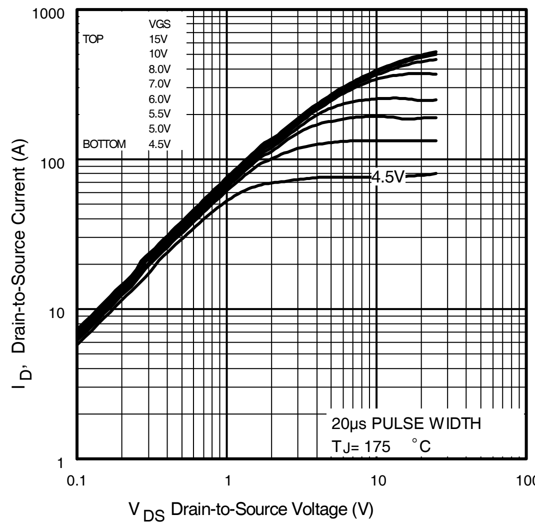


Fig 2. Typical Output Characteristics

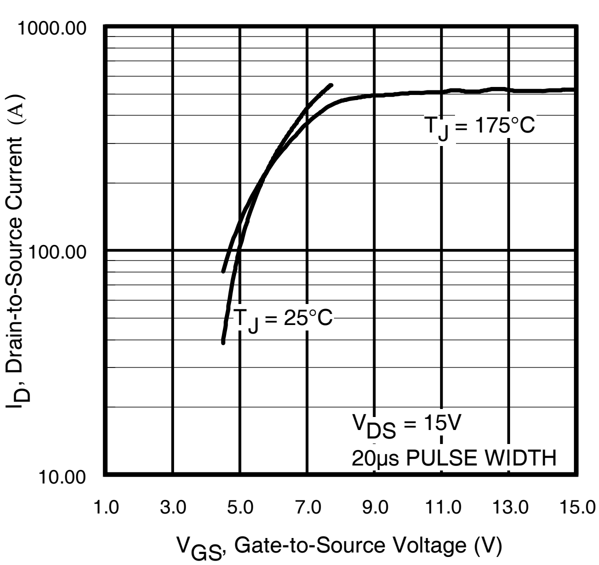


Fig 3. Typical Transfer Characteristics

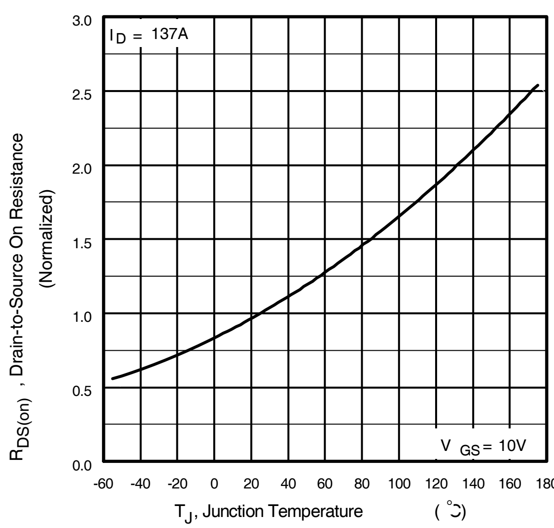


Fig 4. Normalized On-Resistance Vs. Temperature

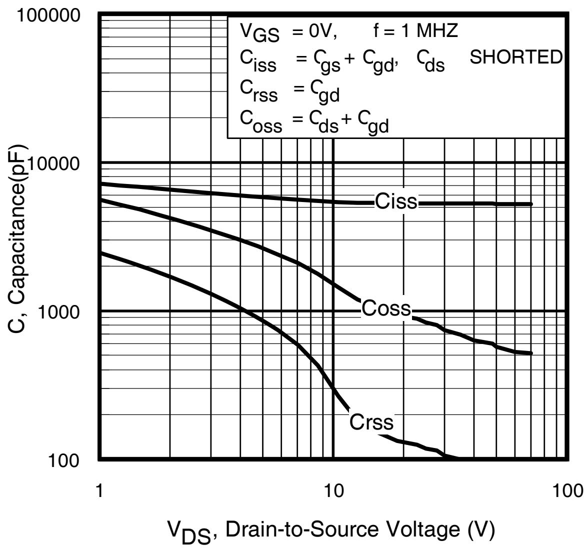


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

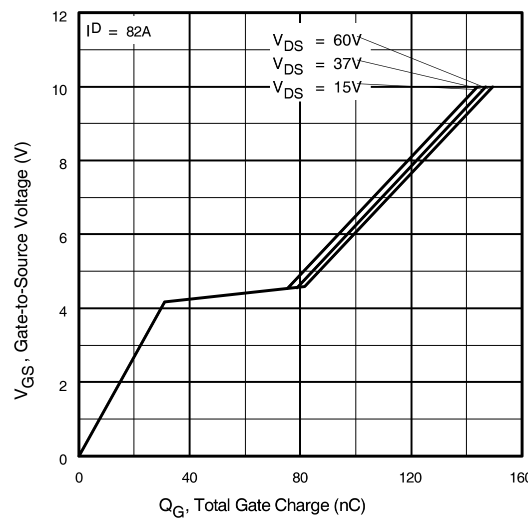


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

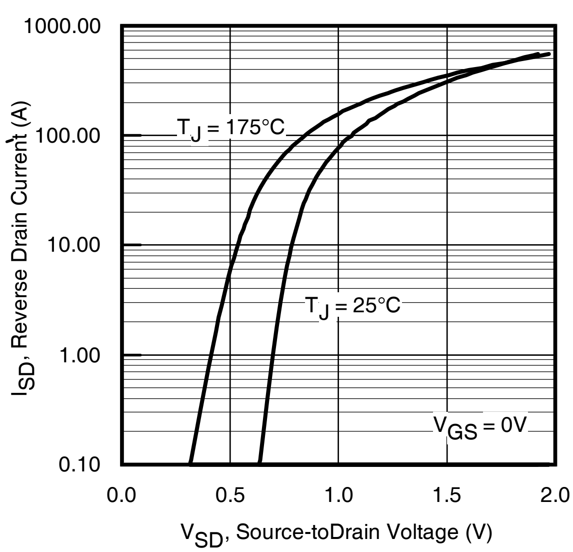


Fig 7. Typical Source-Drain Diode Forward Voltage

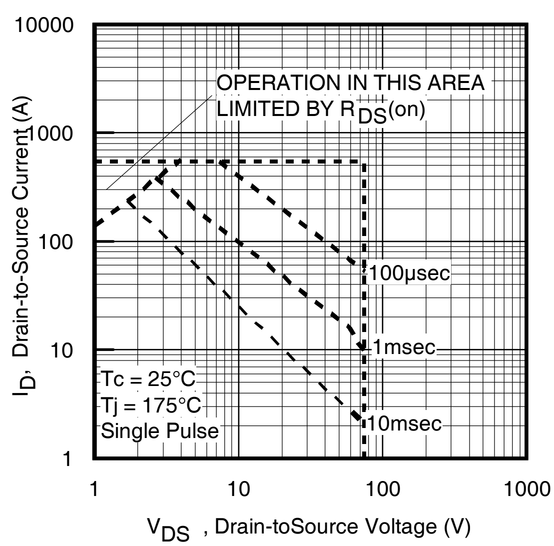


Fig 8. Maximum Safe Operating Area

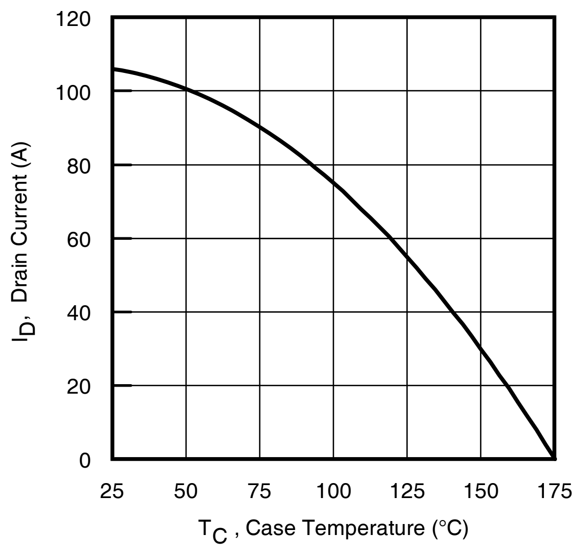


Fig 9. Maximum Drain Current Vs. Case Temperature

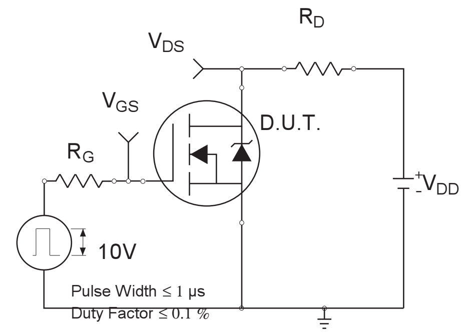


Fig 10a. Switching Time Test Circuit

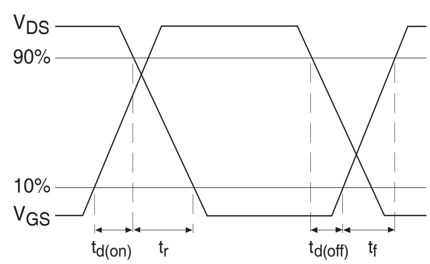


Fig 10b. Switching Time Waveforms

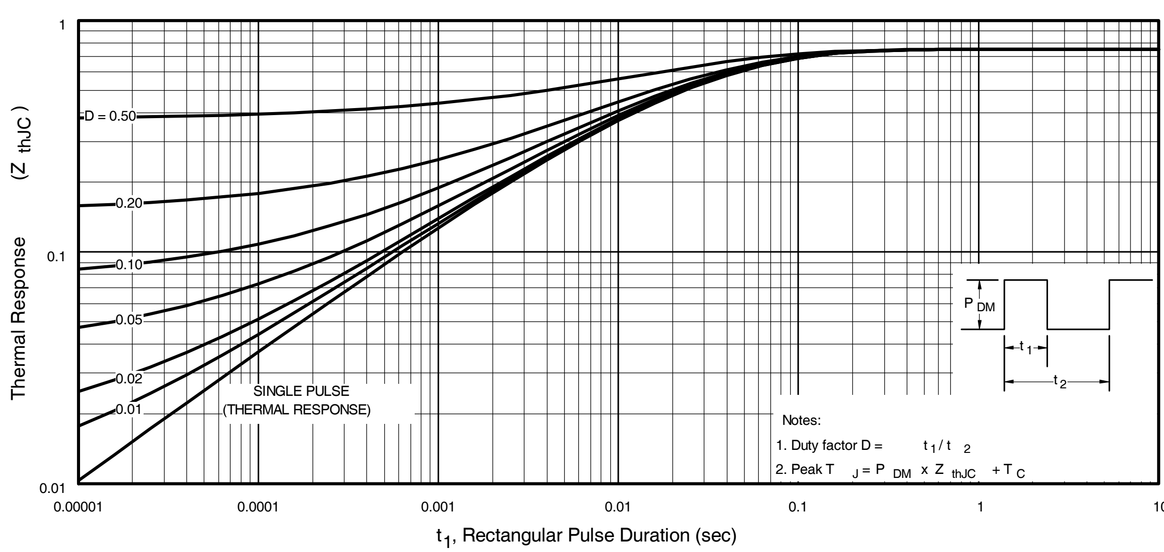


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

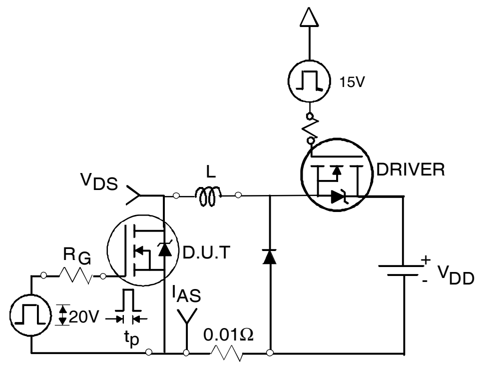
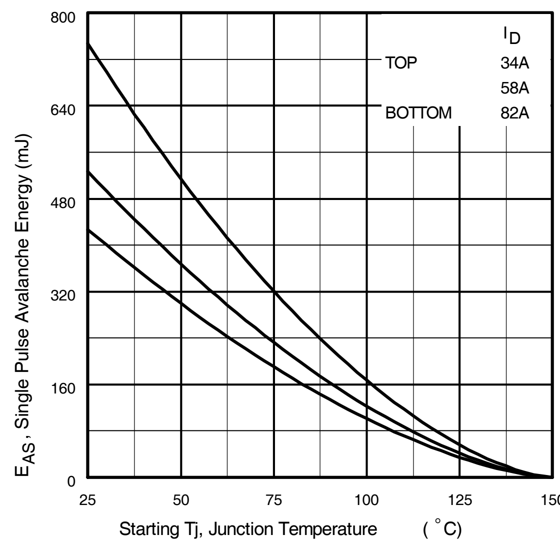


Fig 12a. Unclamped Inductive Test Circuit



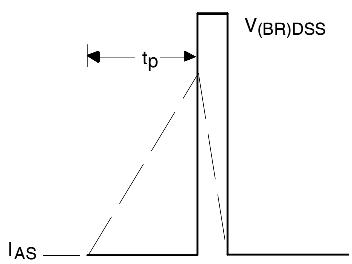


Fig 12b. Unclamped Inductive Waveforms

Fig 12c. Maximum Avalanche Energy Vs. Drain Current

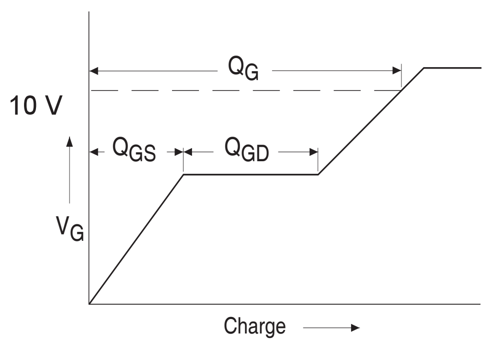


Fig 13a. Basic Gate Charge Waveform

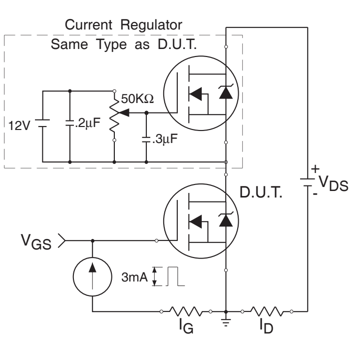


Fig 13b. Gate Charge Test Circuit

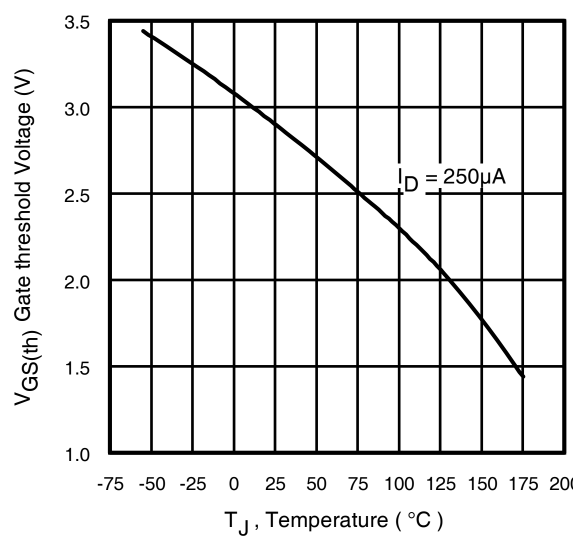


Fig 14. Threshold Voltage Vs. Temperature

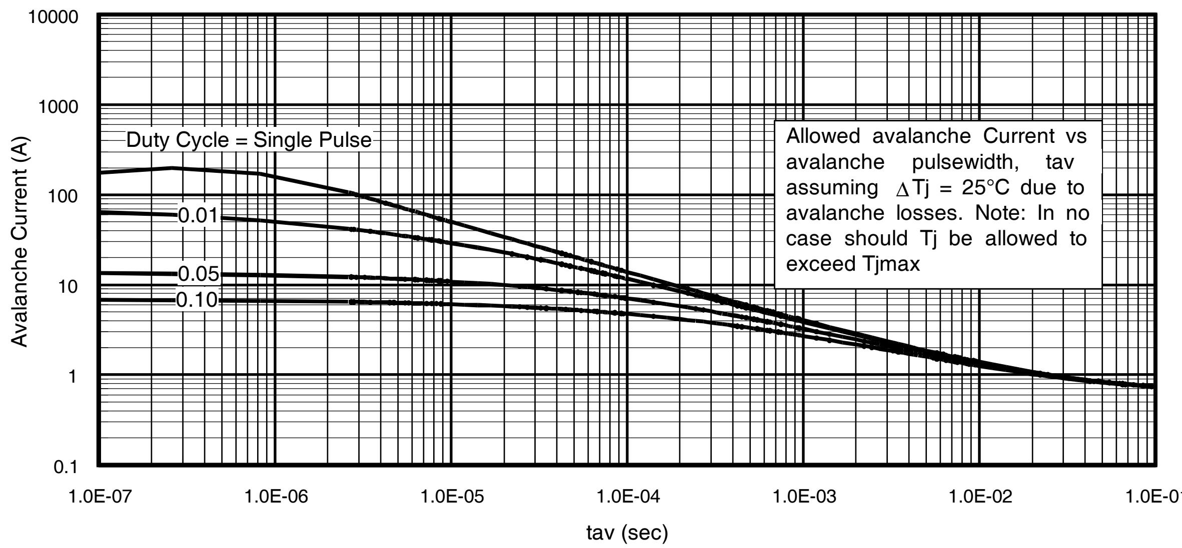


Fig 15. Typical Avalanche Current Vs.Pulsewidth

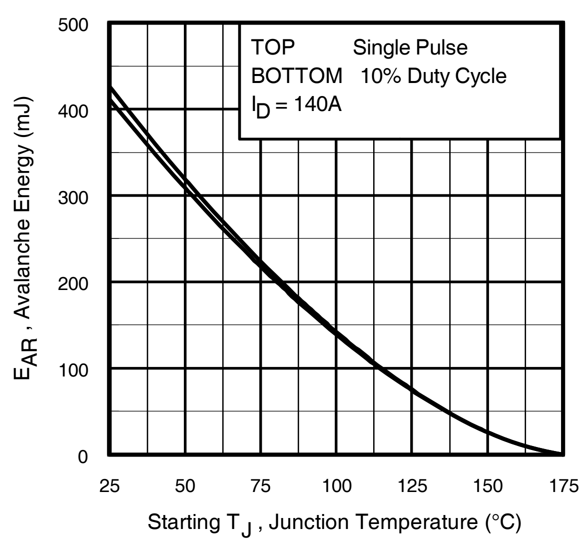


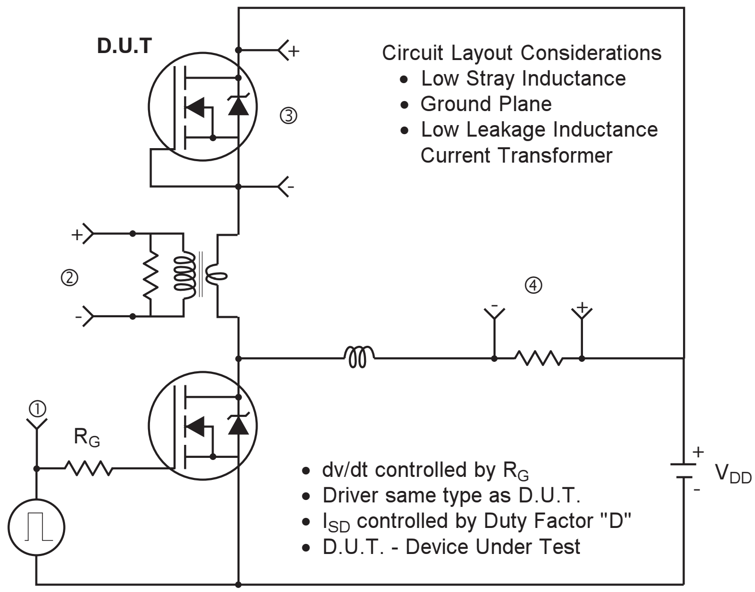
Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

Peak Diode Recovery dv/dt Test Circuit



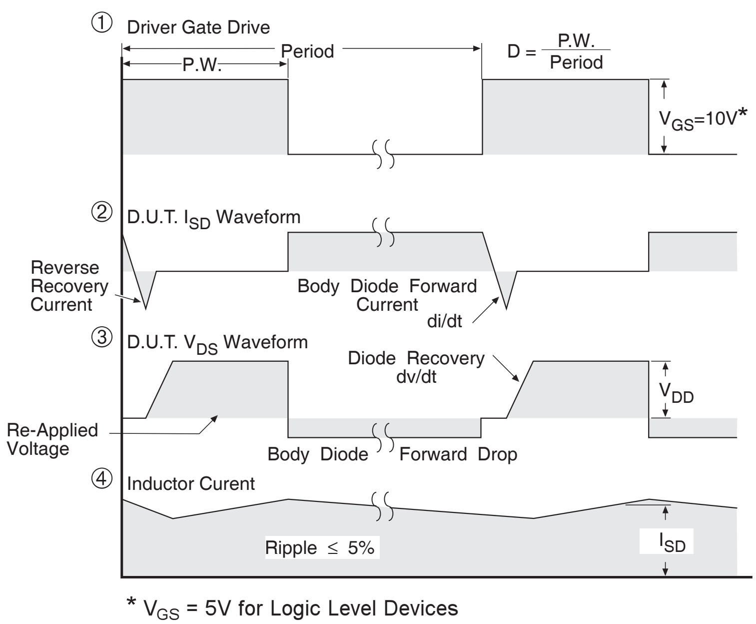
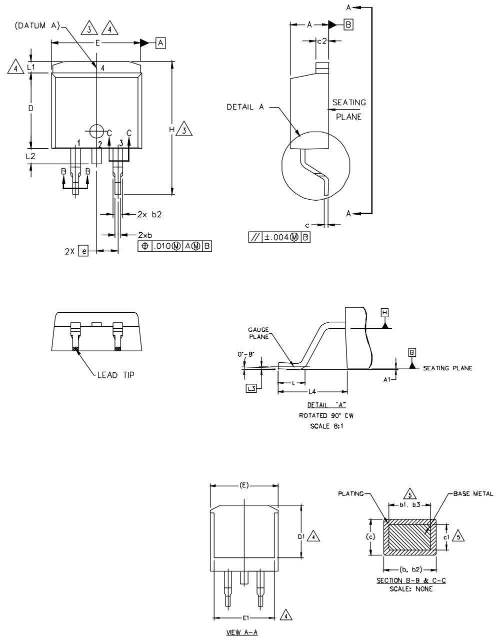


Fig 17. For N-channel HEXFET® power MOSFETs

D2Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270		4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.65	–	.066	4
L2	1.27	1.78	–	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2, 4.– DRAIN
3.– SOURCE

IGBTs, CoPACK

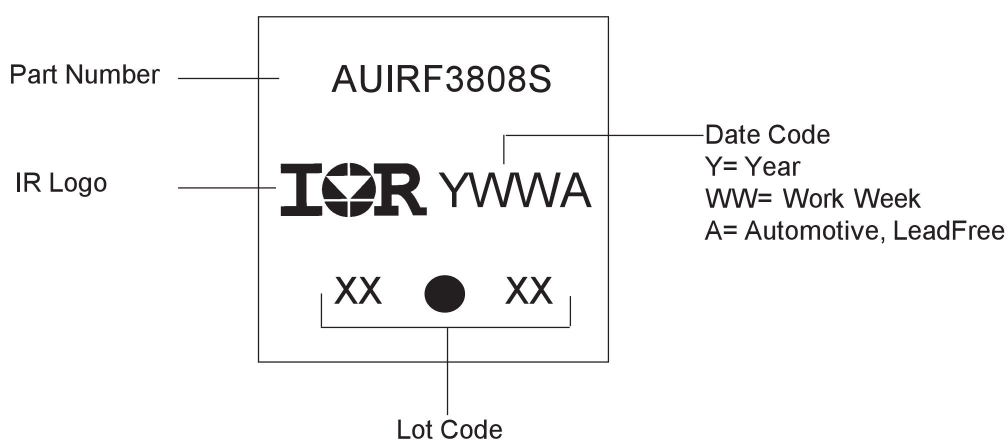
1.– GATE
2, 4.– COLLECTOR
3.– EMITTER

DIODES

1.– ANODE *
2, 4.– CATHODE
3.– ANODE

* PART DEPENDENT.

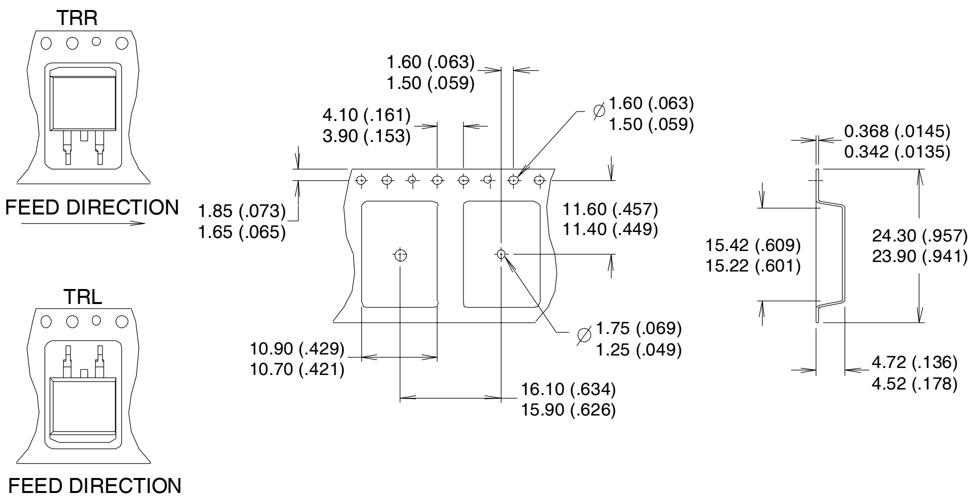
D2Pak (TO-263AB) Part Marking Information

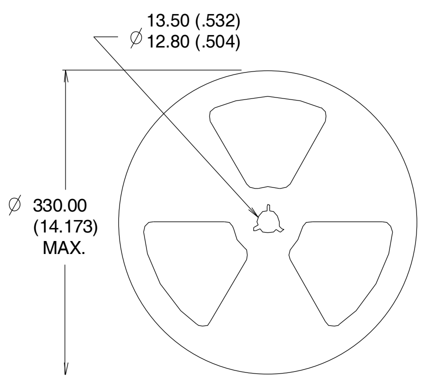


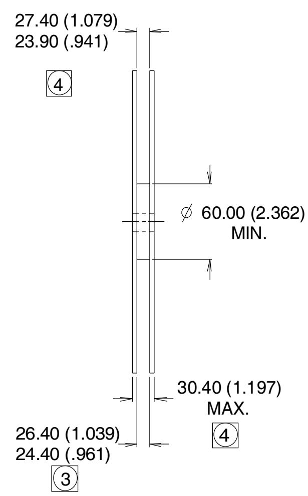
Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

D²Pak (TO-263AB) Tape & Reel Information

Dimensions are shown in millimeters (inches)







NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Ordering Information

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRF3808S	D2Pak	Tube	50	AUIRF3808S
		Tape and Reel Left	800	AUIRF3808STRL
		Tape and Reel Right	800	AUIRF3808STRR

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http://www.irf.com/technical-info/

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