

International
IR Rectifier
RADIATION HARDENED
POWER MOSFET
THRU-HOLE (Low-Ohmic TO-254AA)

PD - 94765

IRHMS57260SE
JANSR2N7476T1
200V, N-CHANNEL
REF: MIL-PRF-19500/685



Product Summary

Part Number	Radiation Level	R _{DS(on)}	ID	QPL Part Number
IRHMS57260SE	100K Rads (Si)	0.044Ω	45A	JANSR2N7476T1



International Rectifier's R5™ technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm²)). The combination of low R_{DS(on)} and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:

- Low R_{DS(on)}
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Ceramic Eyelets
- Electrically Isolated
- Light Weight

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
ID @ VGS = 12V, TC = 25°C	Continuous Drain Current	45	A
ID @ VGS = 12V, TC = 100°C	Continuous Drain Current	29	
IDM	Pulsed Drain Current ①	180	
PD @ TC = 25°C	Max. Power Dissipation	208	W
	Linear Derating Factor	1.67	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	256	mJ
IAR	Avalanche Current ①	45	A
EAR	Repetitive Avalanche Energy ①	20.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	19.8	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Lead Temperature	300 (0.063 in.(1.6 mm from case for 10s))	
	Weight	9.3 (Typical)	g

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	0.25	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.044	Ω	V _{GS} = 12V, I _D = 29A ④
V _{GS(th)}	Gate Threshold Voltage	2.5	—	4.5	V	V _{DS} = V _{GS} , I _D = 1.0mA
g _{fs}	Forward Transconductance	35	—	—	S (Ω)	V _{DS} = 15V, I _{DS} = 29A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	10	μA	V _{DS} = 160V, V _{GS} = 0V
		—	—	25		V _{DS} = 160V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	165	nC	V _{GS} = 12V, I _D = 45A
Q _{gs}	Gate-to-Source Charge	—	—	45		V _{DS} = 100V
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	75		
t _{d(on)}	Turn-On Delay Time	—	—	35	ns	V _{DD} = 100V, I _D = 45A V _{GS} = 12V, R _G = 2.35Ω
t _r	Rise Time	—	—	125		
t _{d(off)}	Turn-Off Delay Time	—	—	80		
t _f	Fall Time	—	—	50		
LS + LD	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm /0.25in. from package) to Source lead (6mm /0.25in. from package) with Source wires internally bonded from Source Pin to Drain Pad
C _{iss}	Input Capacitance	—	5295	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	900	—		
C _{rss}	Reverse Transfer Capacitance	—	37	—		
R _g	Internal Gate Resistance	—	1.47	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	45	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	180		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _j = 25°C, I _S = 45A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	450	ns	T _j = 25°C, I _F = 45A, di/dt ≤ 100A/μs
Q _{RR}	Reverse Recovery Charge	—	—	6.9	μC	V _{DD} ≤ 25V ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	0.60	°C/W	Typical socket mount
R _{thCS}	Case-to-Sink	—	0.21	—		
R _{thJA}	Junction-to-Ambient	—	—	48		

Note: Corresponding Spice and Saber models are available on International Rectifier Web site.

For footnotes refer to the last page

Radiation Characteristics

IRHMS57260SE, JANSR2N7476T1

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	100K Rads (Si)		Units	Test Conditions ③
		Min	Max		
BV _{DSS}	Drain-to-Source Breakdown Voltage	200	—	V	V _{GS} = 0V, I _D = 1.0mA
V _{GS(th)}	Gate Threshold Voltage	2.0	4.5		V _{GS} = V _{DS} , I _D = 1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100		V _{GS} = -20V
I _{DSS}	Zero Gate Voltage Drain Current	—	10	μA	V _{DS} =160V, V _{GS} =0V
R _{DS(on)}	Static Drain-to-Source ④				
	On-State Resistance (TO-3)	—	0.049	Ω	V _{GS} = 12V, I _D = 35A
R _{DS(on)}	Static Drain-to-Source On-state ④ Resistance (Low-Ohmic TO-254)	—	0.044	Ω	V _{GS} = 12V, I _D = 35A
V _{SD}	Diode Forward Voltage ④	—	1.2	V	V _{GS} = 0V, I _D = 45A

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET MeV/(mg/cm ²)	Energy (MeV)	Range (μm)	V _{DS} (V)				
				@V _{GS} =0V	@V _{GS} =-5V	@V _{GS} =-10V	@V _{GS} =-15V	@V _{GS} =-20V
Br	37	305	39	200	200	200	200	200
I	60	340	32	200	200	200	185	120
Au	82	350	28	200	200	150	50	25

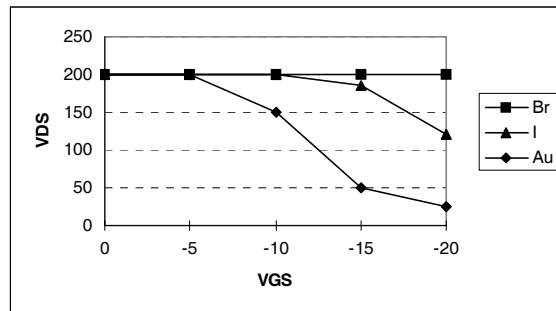
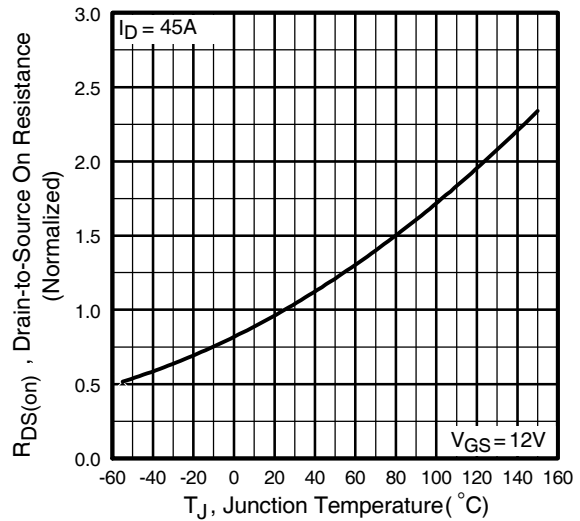
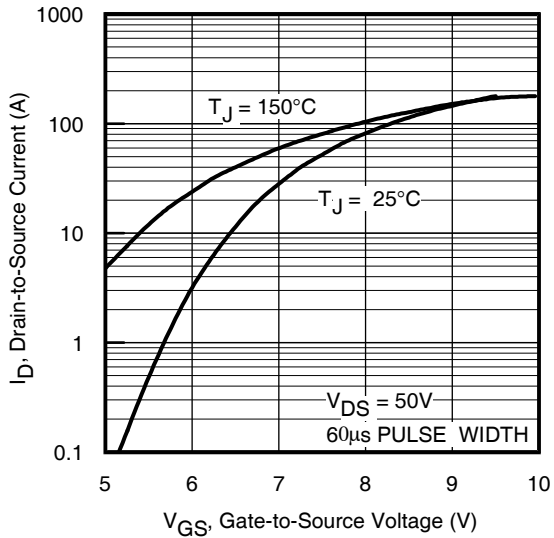
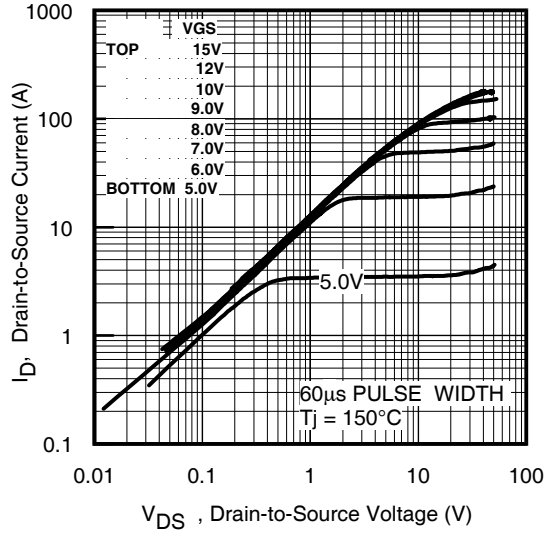
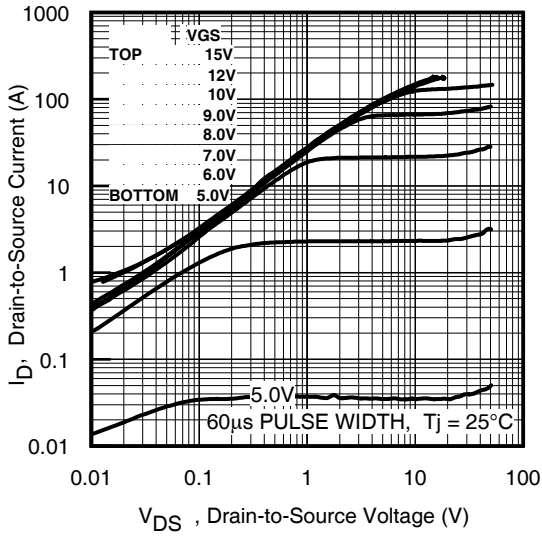


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page



Pre-Irradiation

IRHMS57260SE, JANSR2N7476T1

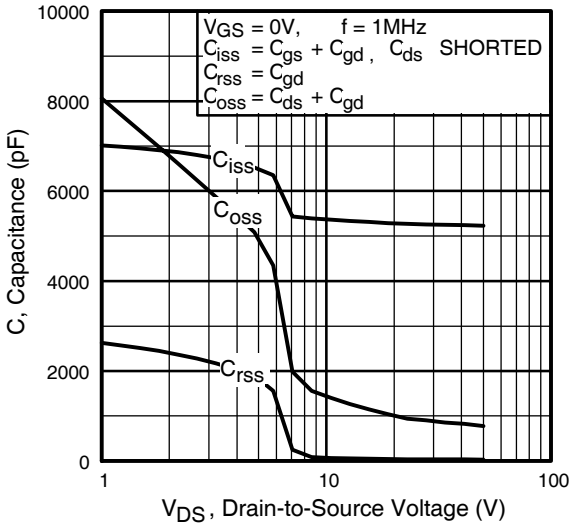


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

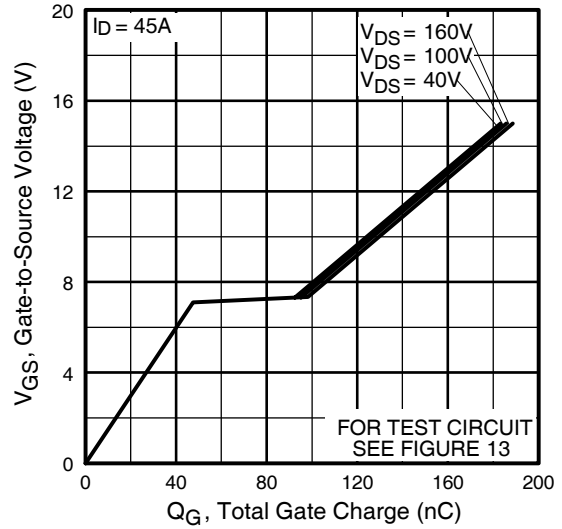


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

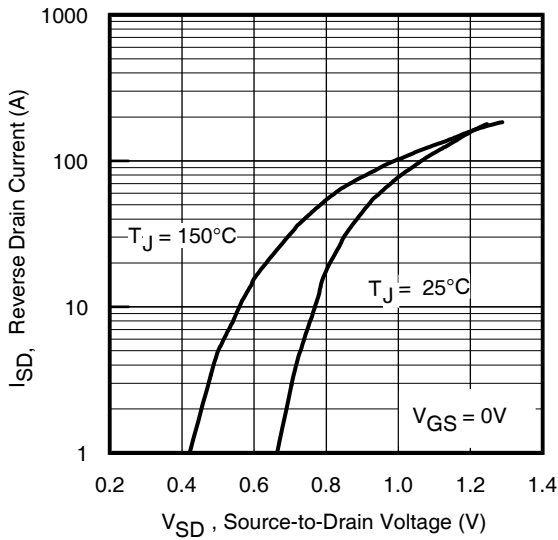


Fig 7. Typical Source-Drain Diode Forward Voltage

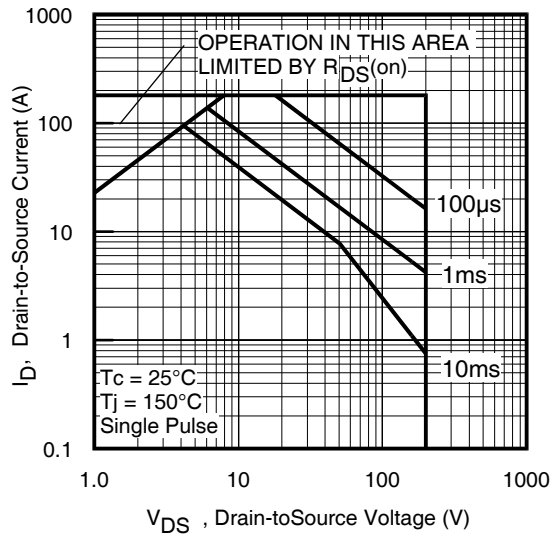


Fig 8. Maximum Safe Operating Area

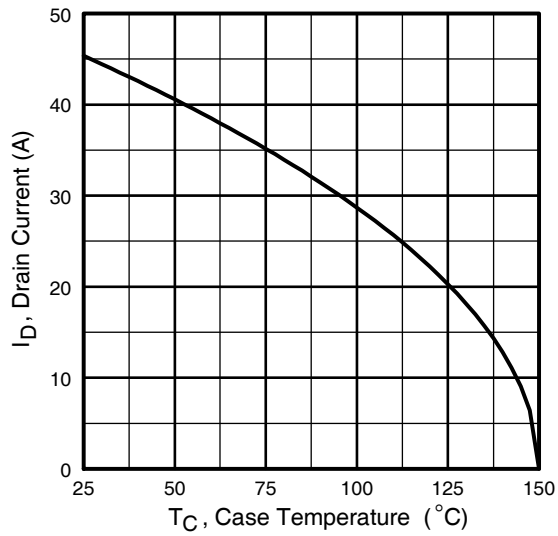


Fig 9. Maximum Drain Current Vs. Case Temperature

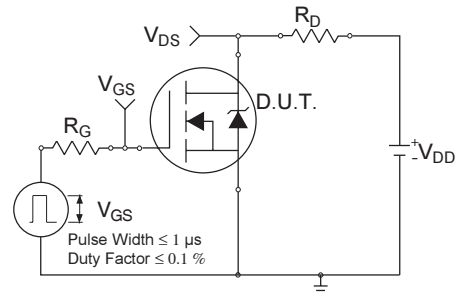


Fig 10a. Switching Time Test Circuit

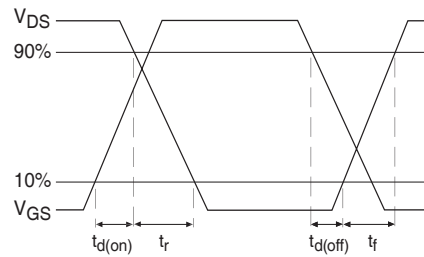


Fig 10b. Switching Time Waveforms

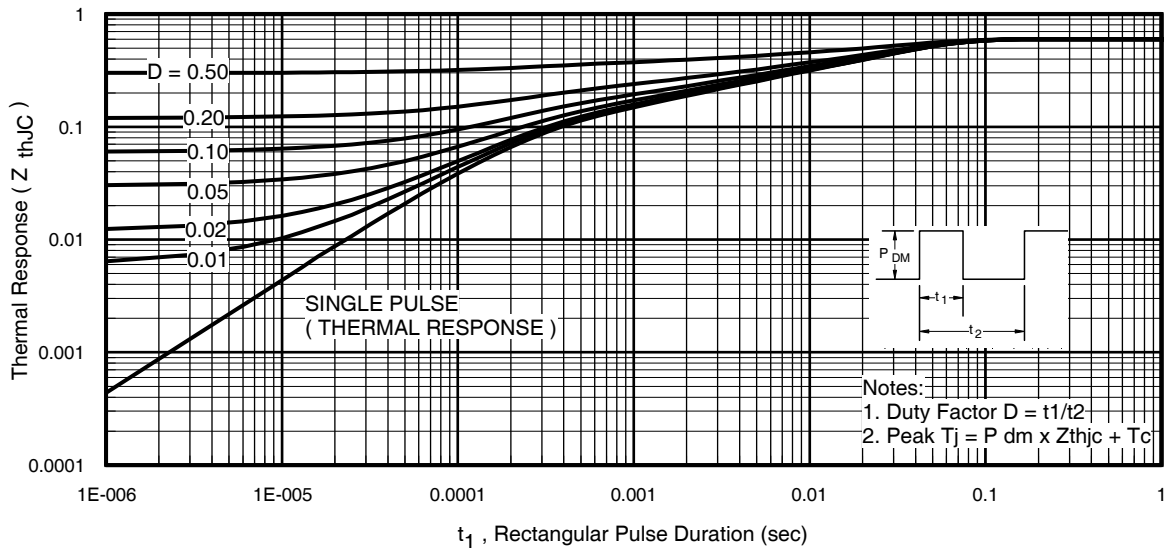


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Pre-Irradiation

IRHMS57260SE, JANSR2N7476T1

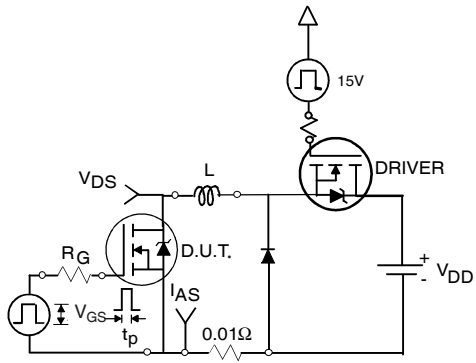


Fig 12a. Unclamped Inductive Test Circuit

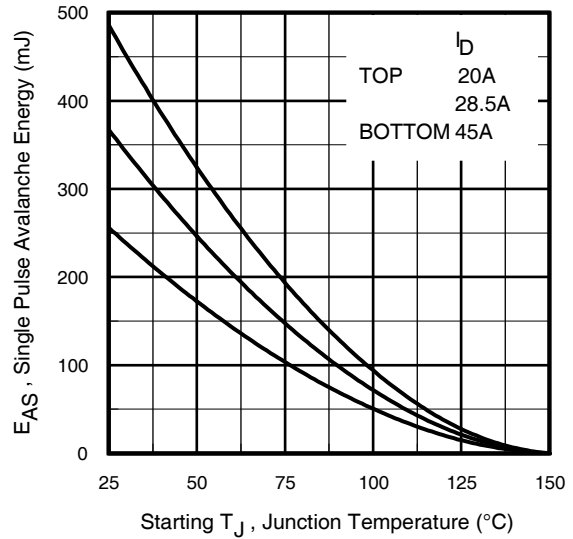


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

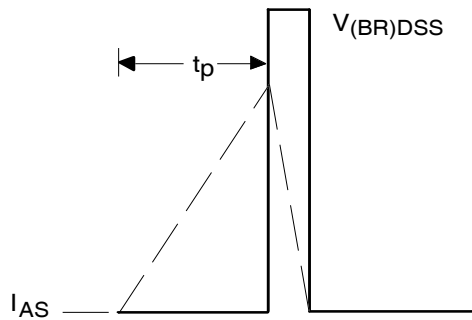


Fig 12b. Unclamped Inductive Waveforms

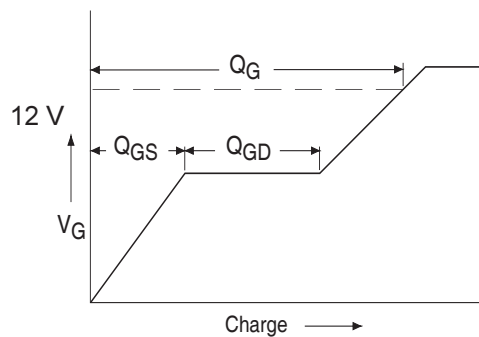


Fig 13a. Basic Gate Charge Waveform

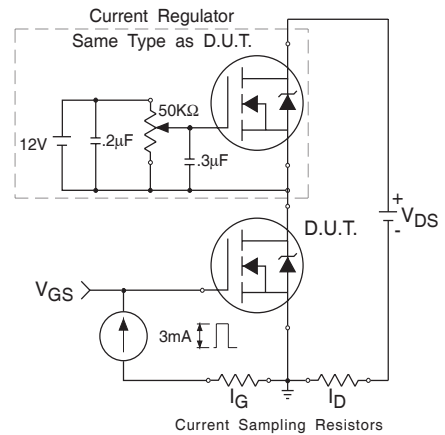


Fig 13b. Gate Charge Test Circuit

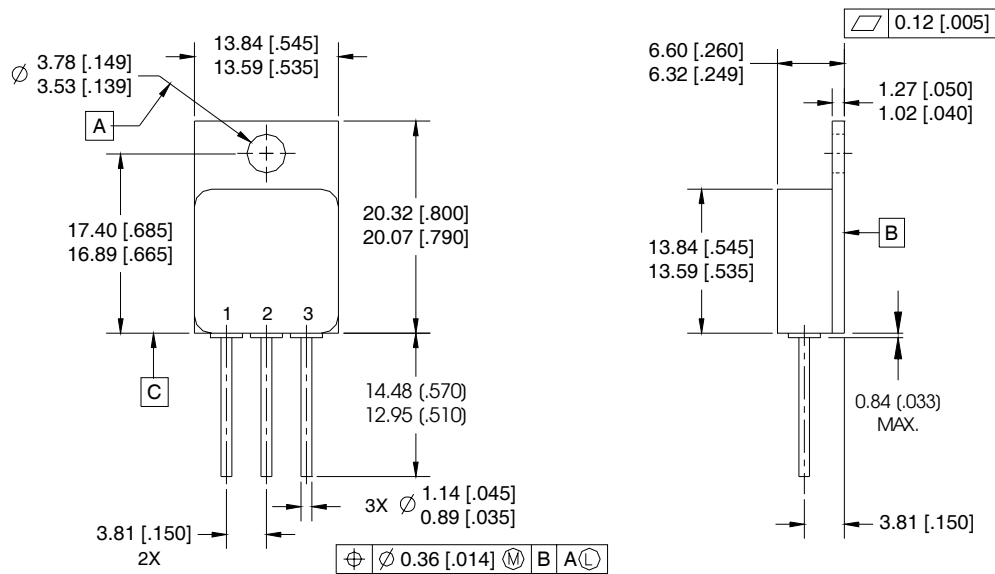
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Pre-Irradiation

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 50V$, starting $T_J = 25^\circ C$, $L = 0.25mH$
Peak $I_L = 45A$, $V_{GS} = 12V$
- ③ $I_{SD} \leq 45A$, $di/dt \leq 375A/\mu s$,
 $V_{DD} \leq 200V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$
- ⑤ **Total Dose Irradiation with V_{GS} Bias.**
12 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.**
160 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — Low-Ohmic TO-254AA



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-254AA.

PIN ASSIGNMENTS

- 1 = DRAIN
- 2 = SOURCE
- 3 = GATE

CAUTION

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR LEOMINSTER : 205 Crawford St., Leominster, Massachusetts 01453, USA Tel: (978) 534-5776
TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.

Data and specifications subject to change without notice. 09/2004