Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

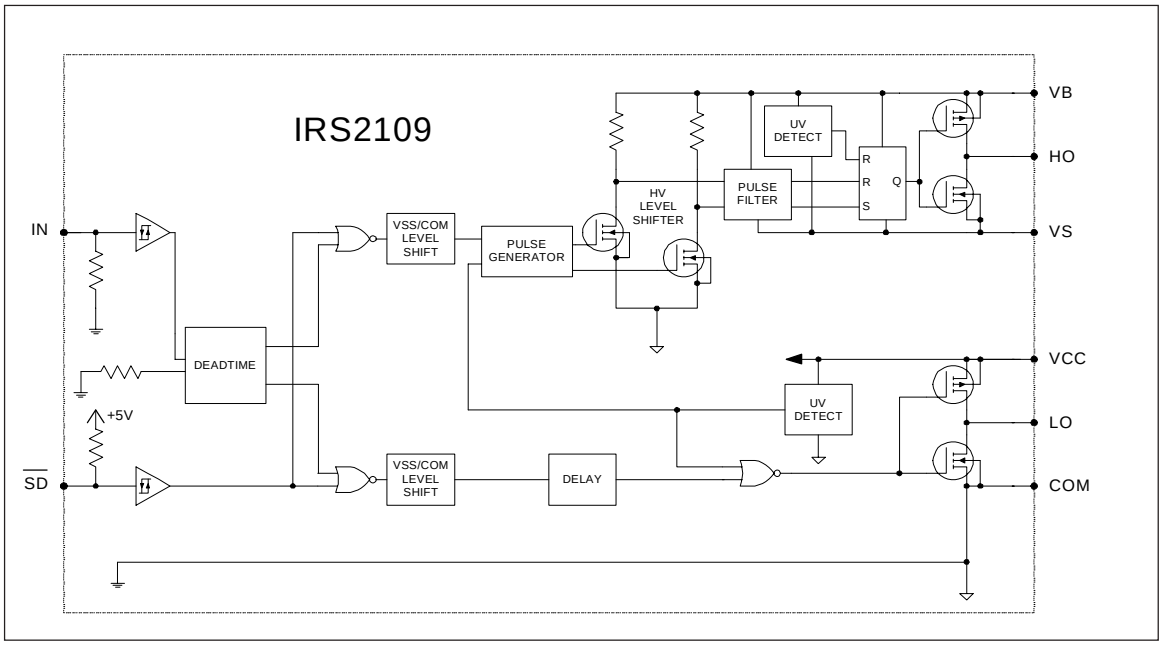
Symbol	Definition		Min.	Max.	Units
V_B	High-side floating absolute voltage		-0.3	625	V
V_S	High-side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High-side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low-side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low-side output voltage		-0.3	V_{CC} + 0.3	
DT	Programmable deadtime pin voltage (IRS21094 only)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{SS}	Logic ground (IRS21094 only)		V_{CC} -25	V_{CC} +0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25$ °C	(8 Lead PDIP)	—	1.0	W
		(8 Lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8 Lead PDIP)	—	125	°C/W
		(8 Lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

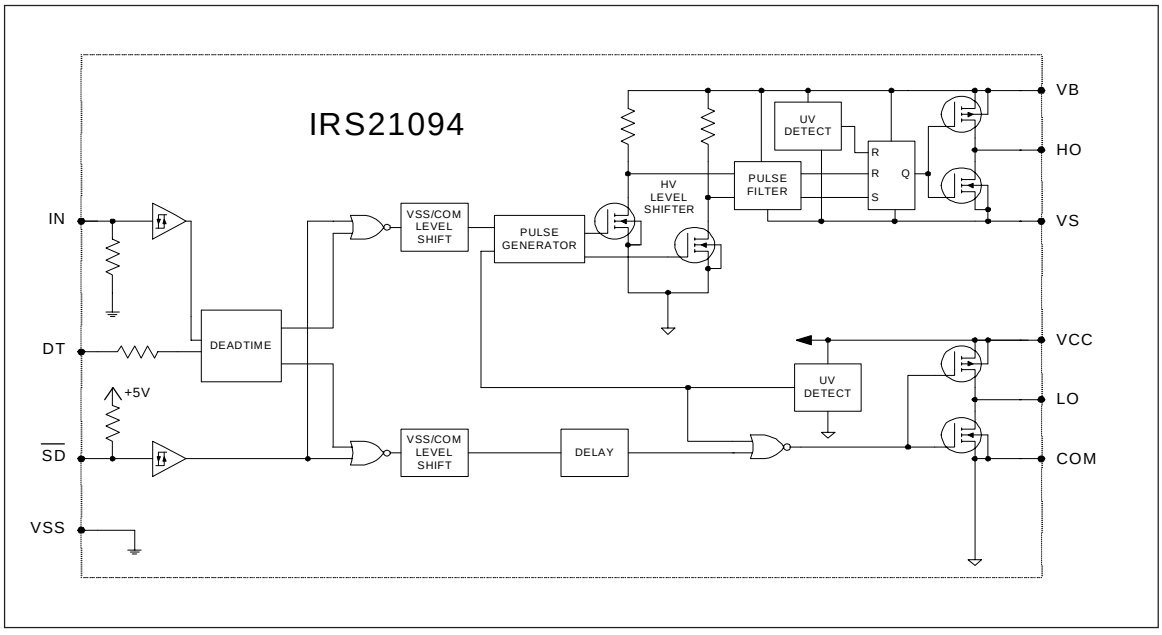
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM, DT= V_{SS} and T_A = 25 °C unless otherwise specified. The V_{IL}, V_{IH}, and I_{IN} parameters are referenced to V_{SS} /COM and are applicable to the respective input leads: IN and $\overline{SD}$. The V_O, I_O, and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” input voltage for HO & logic “0” for LO	2.5	—	—	V	V_{CC} = 10 V to 20 V
V_{IL}	Logic “0” input voltage for HO & logic “1” for LO	—	—	0.8		
$V_{SD,TH+}$	$\overline{SD}$ input positive going threshold	2.5	—	—		
$V_{SD,TH-}$	$\overline{SD}$ input negative going threshold	—	—	0.8		
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.05	0.2		I_O = 2 mA
V_{OL}	Low level output voltage, V_O	—	0.02	0.1		
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	20	75	130		V_{IN} = 0 V or 5 V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	V_{IN} = 0 V or 5 V R_{DT} = 0 Ω
I_{IN+}	Logic “1” input bias current	—	5	20	µA	IN = 5 V, $\overline{SD}$ = 0 V
I_{IN-}	Logic “0” input bias current	—	—	2		IN = 0 V, $\overline{SD}$ = 5 V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	120	290	—	mA	V_O = 0 V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	250	600	—		V_O = 15 V,PW ≤ 10 µs

Functional Block Diagrams





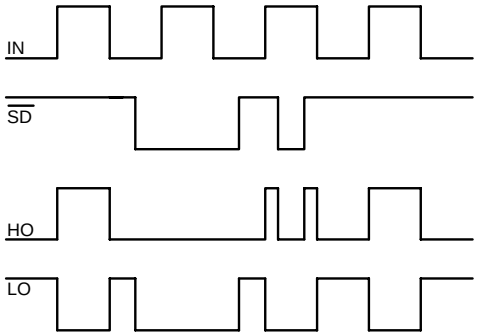


Figure 1. Input/Output Timing Diagram

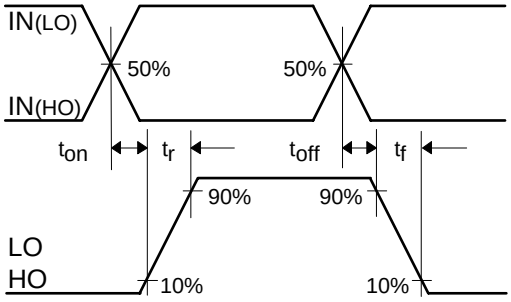


Figure 2. Switching Time Waveform Definitions

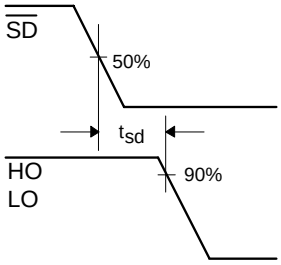


Figure 3. Shutdown Waveform Definitions

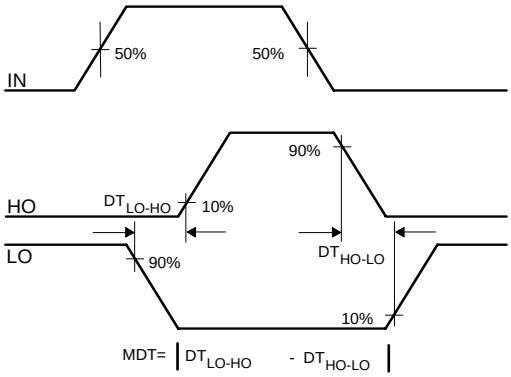


Figure 4. Deadtime Waveform Definitions

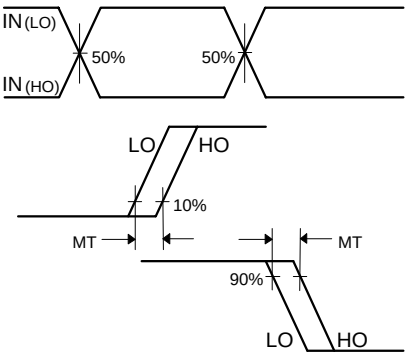


Figure 5. Delay Matching Waveform Definitions

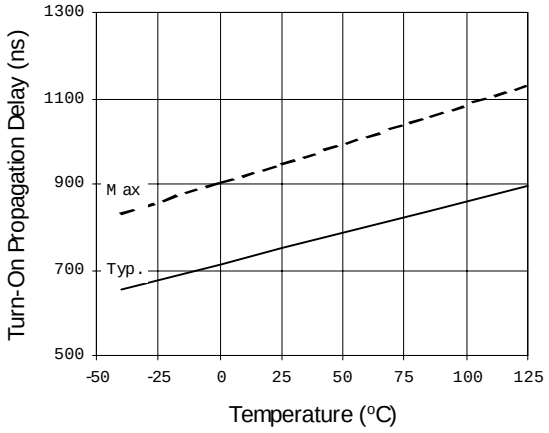


Figure 6A. Turn-On Propagation Delay vs. Temperature

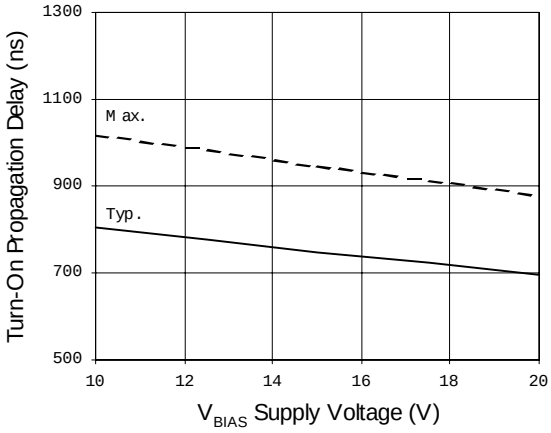


Figure 6B. Turn-On Propagation Delay vs. Supply Voltage

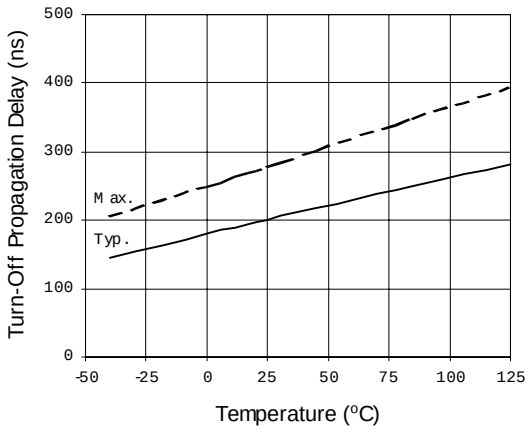


Figure 7A. Turn-Off Propagation Delay vs. Temperature

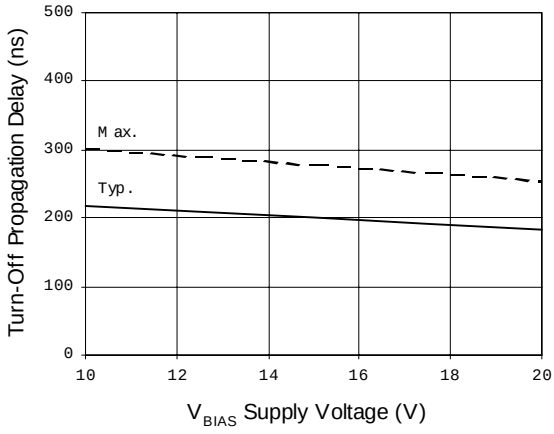


Figure 7B. Turn-Off Propagation Delay vs. Supply Voltage

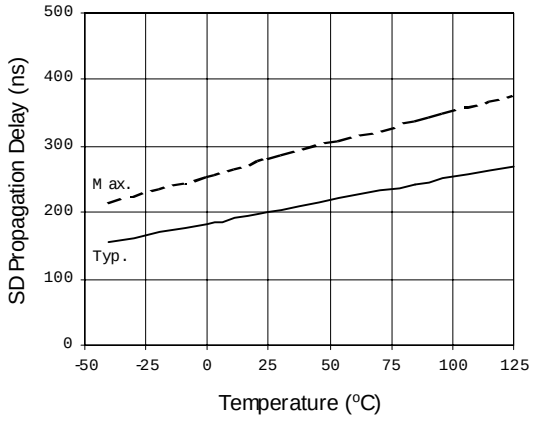


Figure 8A. SD Propagation Delay vs. Temperature

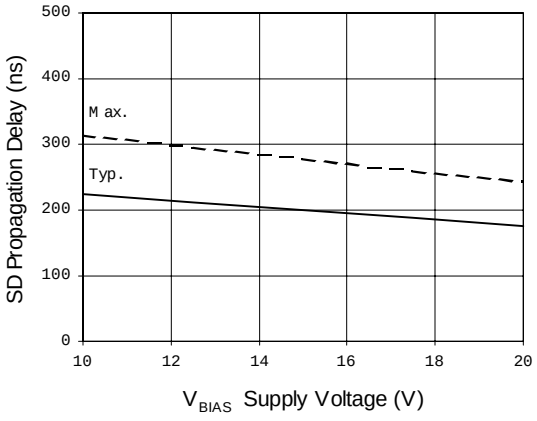


Figure 8B. SD Propagation Delay vs. Supply Voltage

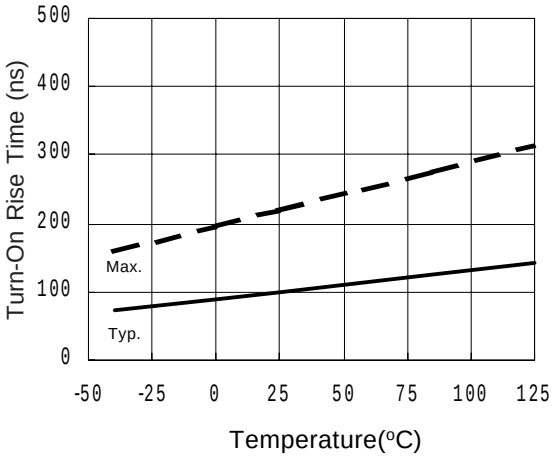


Figure 9A. Turn-On Rise Time vs. Temperature

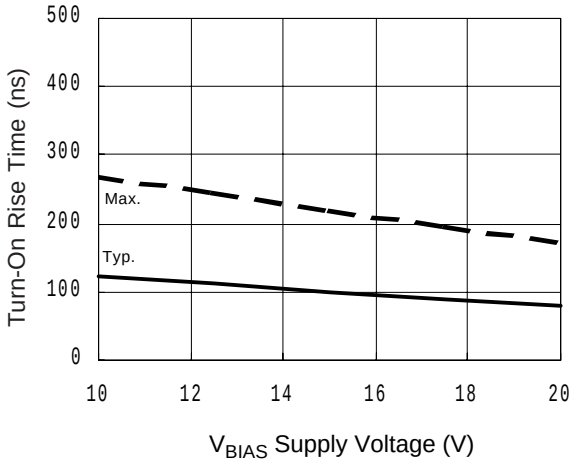


Figure 9B. Turn-On Rise Time vs. Supply Voltage

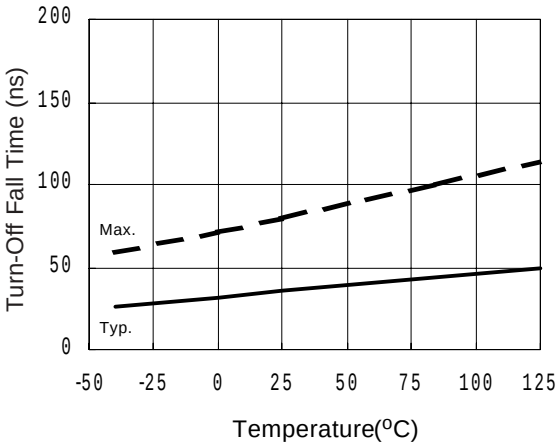


Figure 10A. Turn-Off Fall Time vs. Temperature

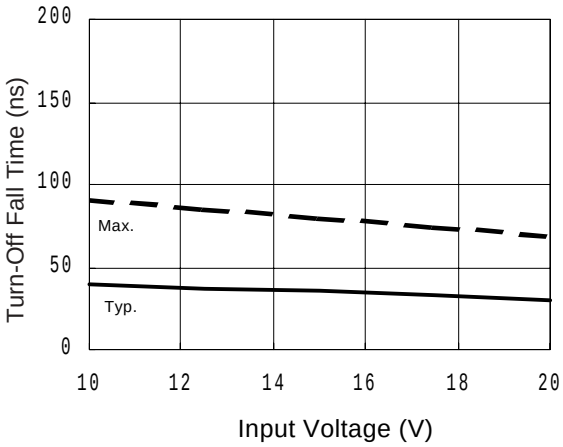


Figure 10B. Turn-Off Fall Time vs. Supply Voltage

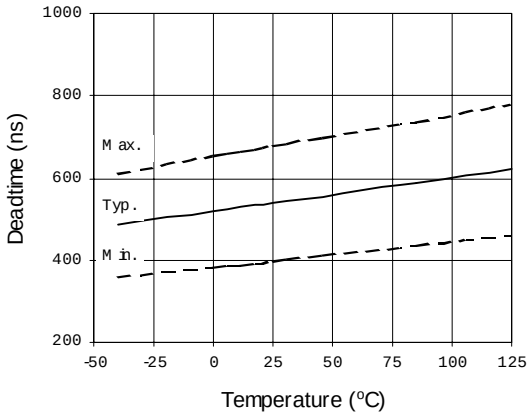


Figure 11A. Deadtime vs. Temperature

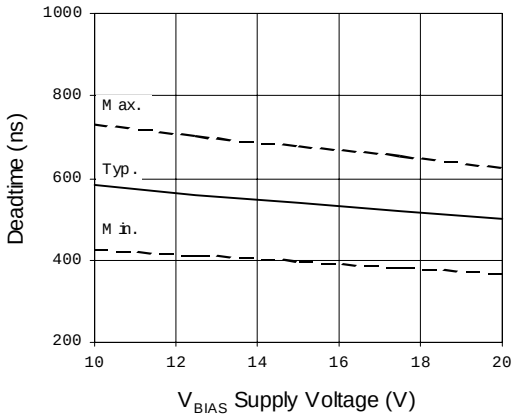


Figure 11B. Deadtime vs. Supply Voltage

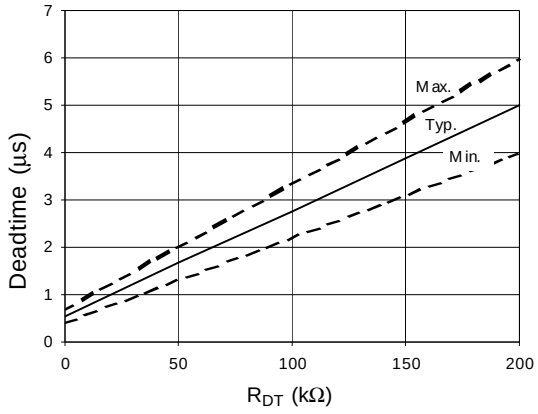


Figure 11C. Deadtime vs. R_{DT} (IR21094 only)

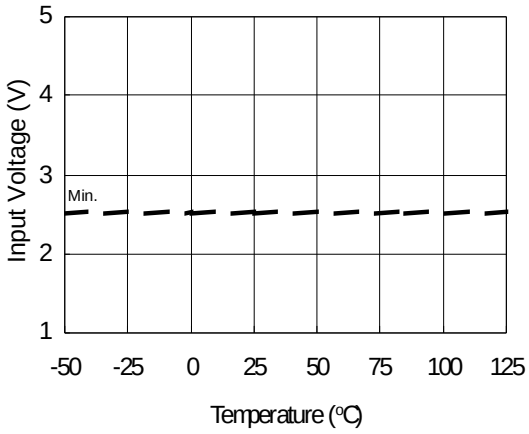


Figure 12A. Logic "1" Input Voltage vs. Temperature

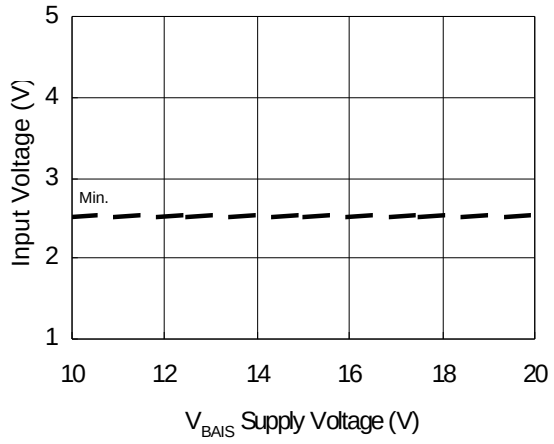


Figure 12B. Logic "1" Input Voltage vs. Supply Voltage

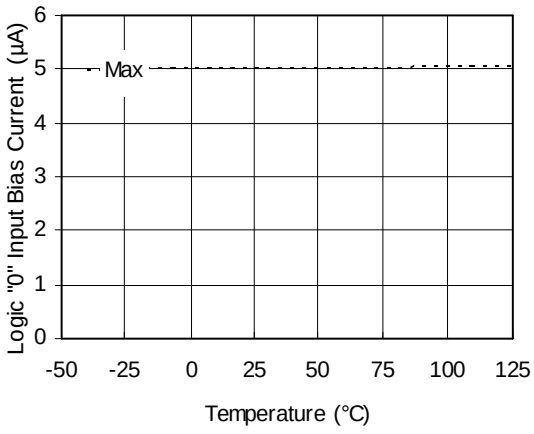


Figure 13A. Logic "0" Input Bias Current vs. Temperature

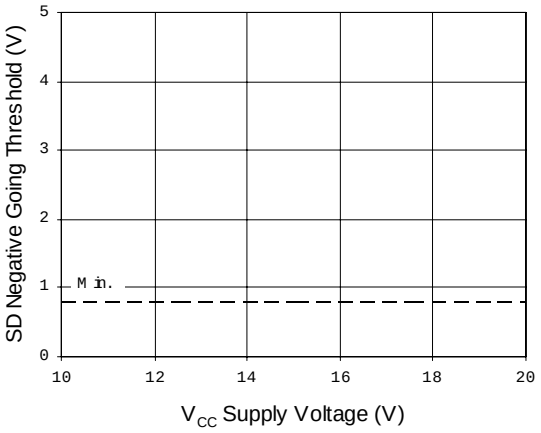


Figure 15B. SD Negative Going Threshold vs. Supply Voltage

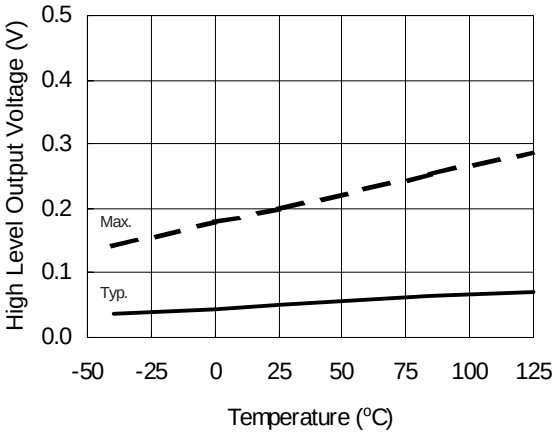


Figure 16A. High Level Output Voltage vs. Temperature

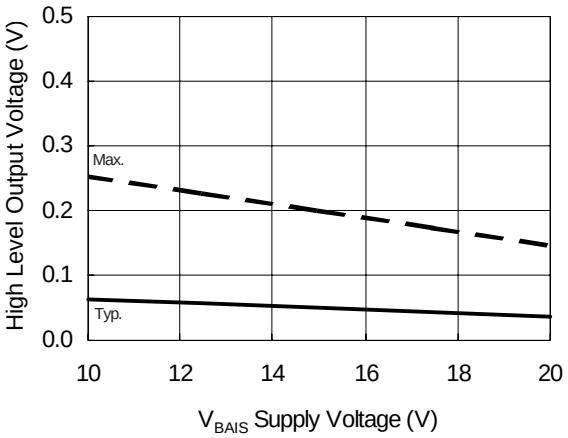


Figure 16B. High Level Output Voltage vs. Supply Voltage

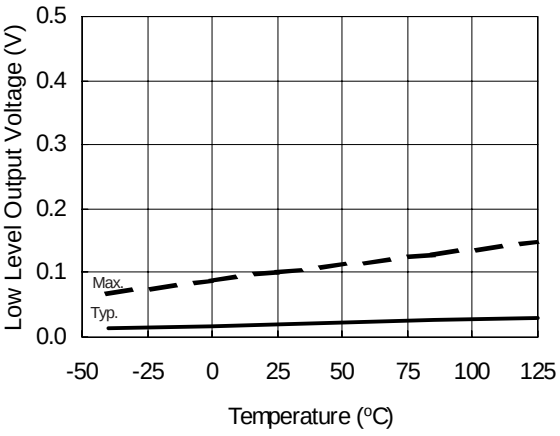


Figure 17A. Low Level Output Voltage vs. Temperature

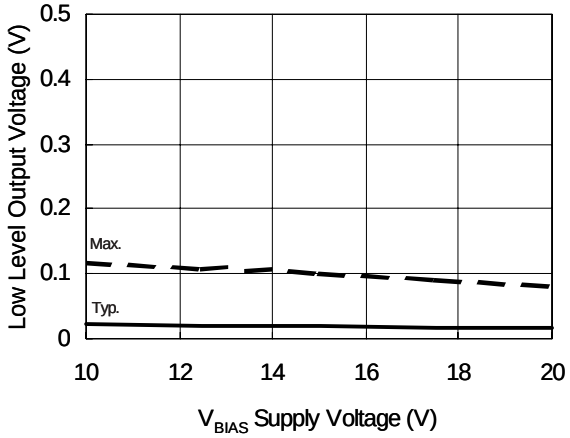


Figure 17B. Low Level Output Voltage vs. Supply Voltage

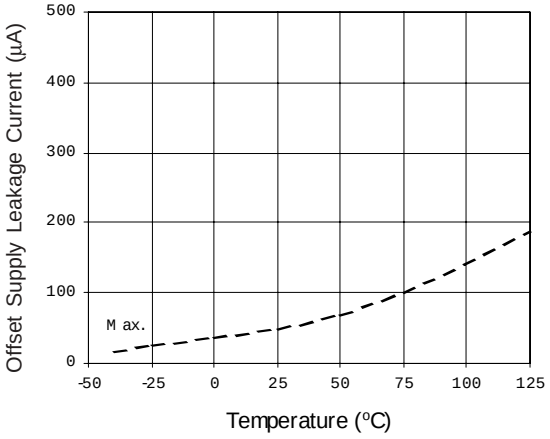


Figure 18A. Offset Supply Leakage Current vs. Temperature

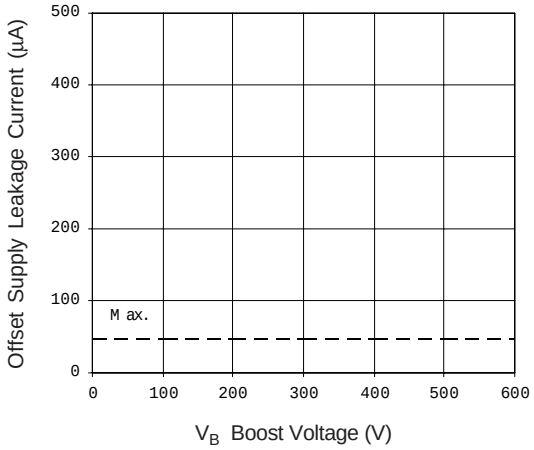


Figure 18B. Offset Supply Leakage Current vs. Boost Voltage

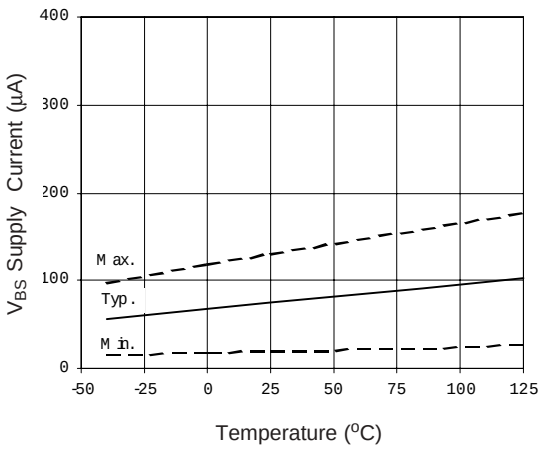


Figure 19A. V_{BS} Supply Current vs. Temperature

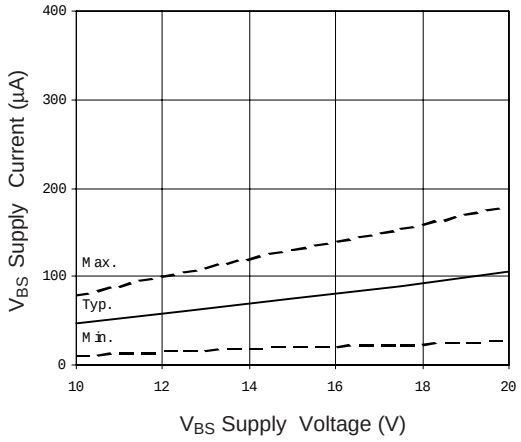


Figure 19B. V_{BS} Supply Current vs. Supply Voltage

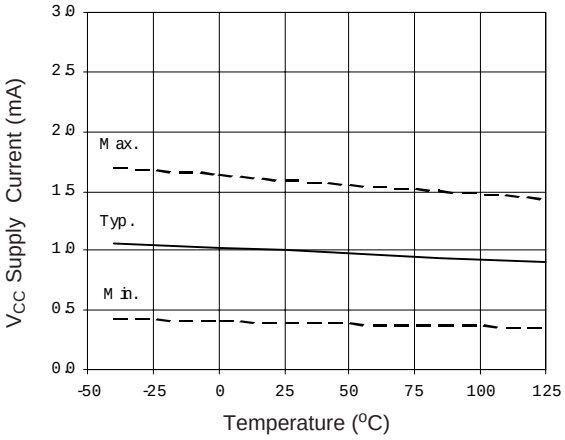


Figure 20A. V_{CC} Supply Current vs. Temperature

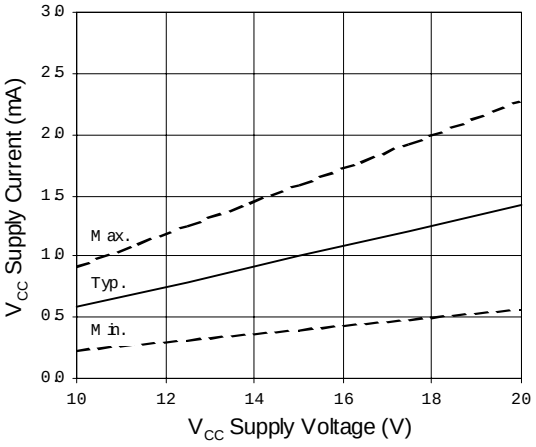


Figure 20B. V_{CC} Supply Current vs. V_{CC} Supply Voltage

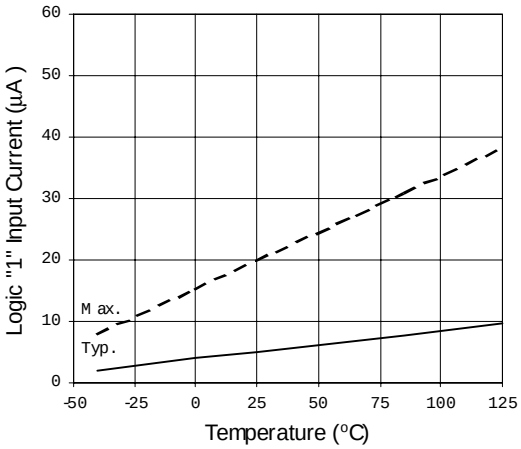


Figure 21A. Logic "1" Input Current vs. Temperature

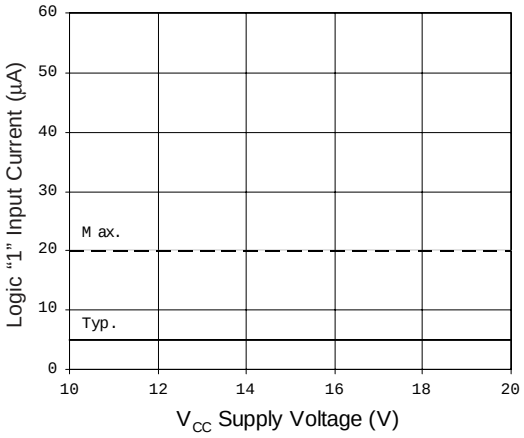


Figure 21B. Logic "1" Input Current vs. Supply Voltage

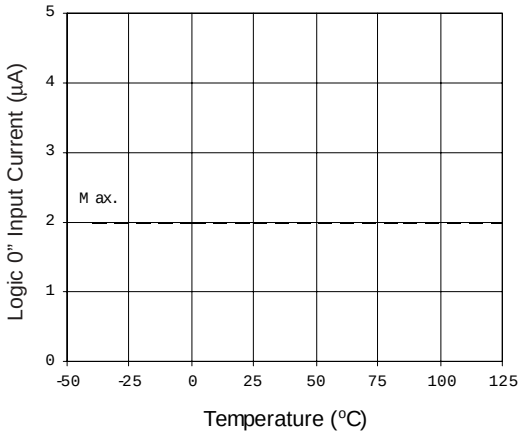


Figure 22A. Logic "0" Input Current vs. Temperature

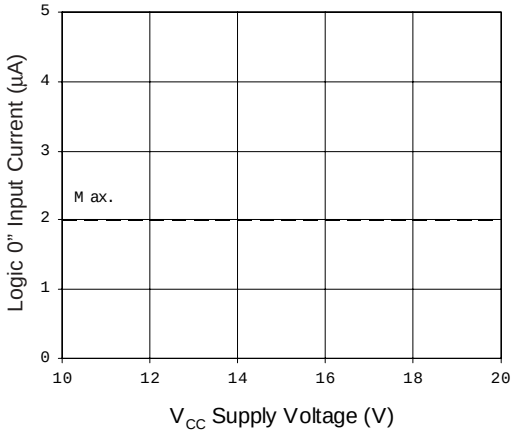


Figure 22B. Logic "0" Input Currentt vs. Supply Voltage

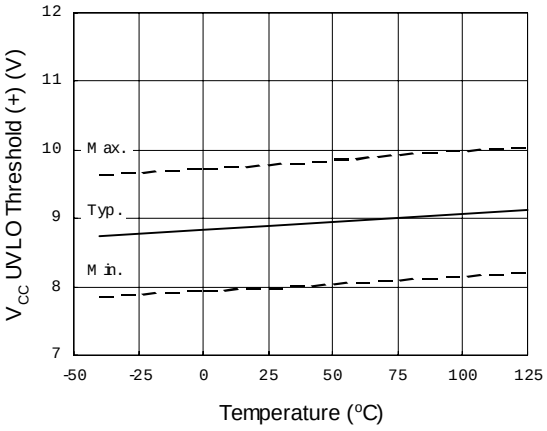


Figure 23. V_{CC} Undervoltage Threshold (+) vs. Temperature

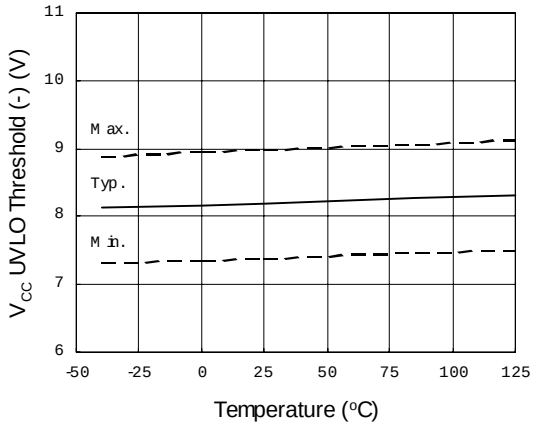


Figure 24. V_{CC} Undervoltage Threshold (-) vs. Temperature

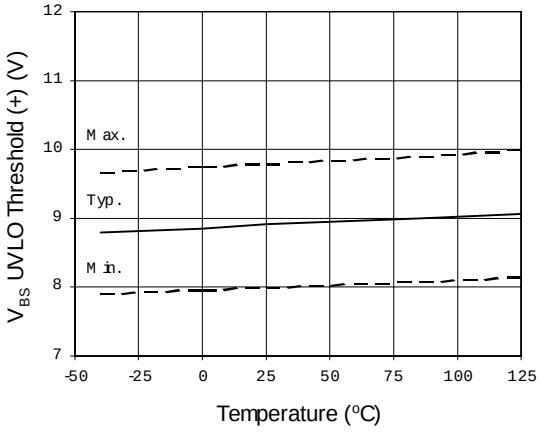


Figure 25. V_{BS} Undervoltage Threshold (+) vs. Temperature

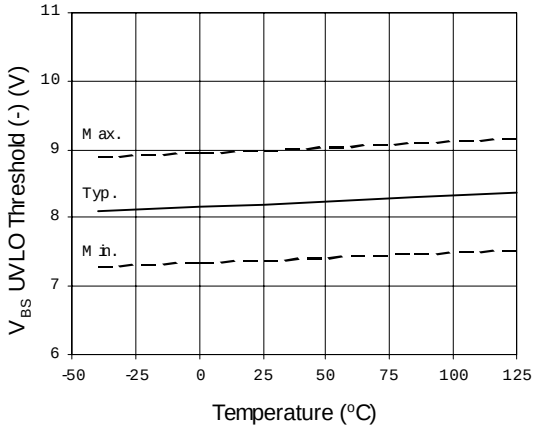


Figure 26. V_{BS} Undervoltage Threshold (-) vs. Temperature

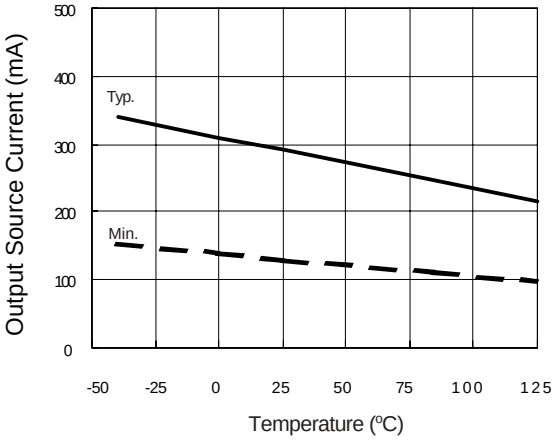


Figure 27A. Output Source Current vs. Temperature

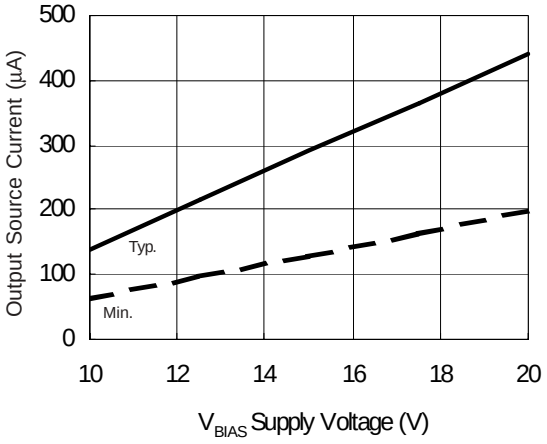


Figure 27B. Output Source Current vs. Supply Voltage

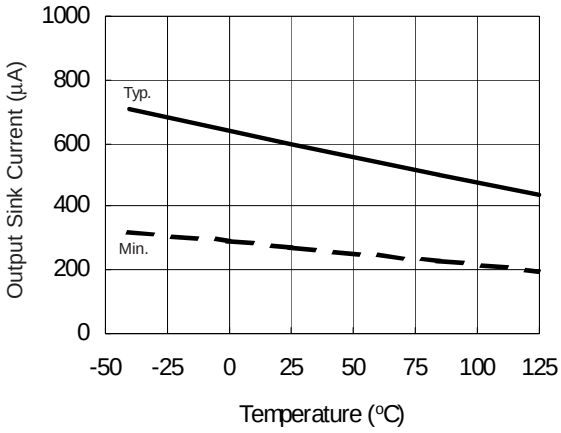


Figure 28A. Output Sink Current vs. Temperature

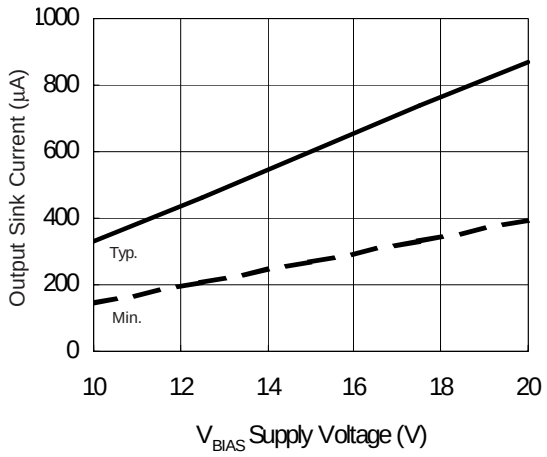


Figure 28B. Output Sink Currentt vs. Supply Voltage

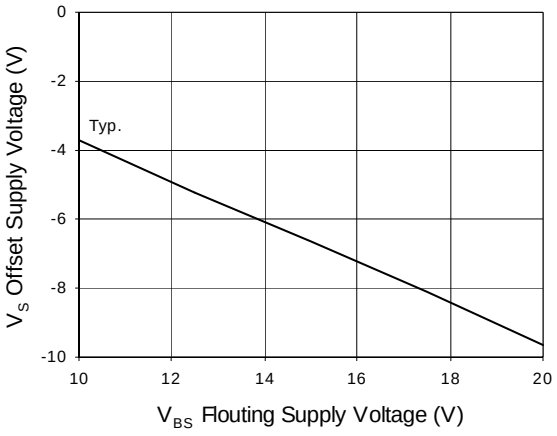


Figure 29. Maximum V_S Negative Offset vs. Supply Voltage

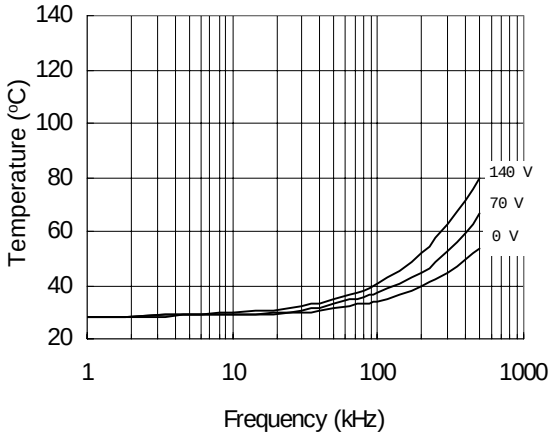


Figure 30. IRS2109 vs Frequency (IRFBC20)
R_{gate} = 33 Ω, V_{CC} = 15 V

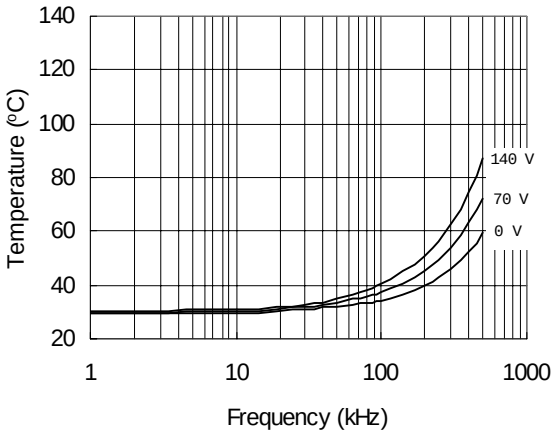


Figure 31. IRS2109 vs Frequency (IRFBC30)
R_{gate} = 22 Ω, V_{CC} = 15 V

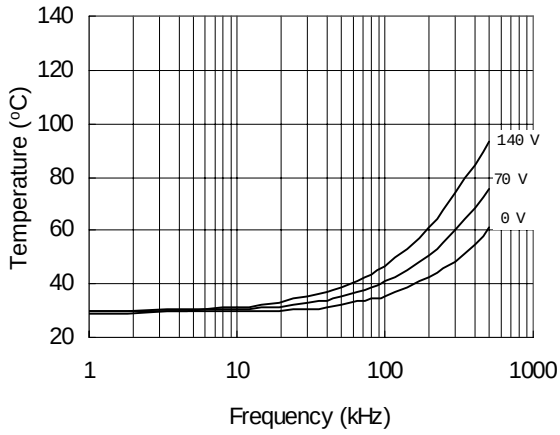


Figure 32. IRS2109 vs Frequency (IRFBC40)
R_{gate} = 15 Ω, V_{CC} = 15 V

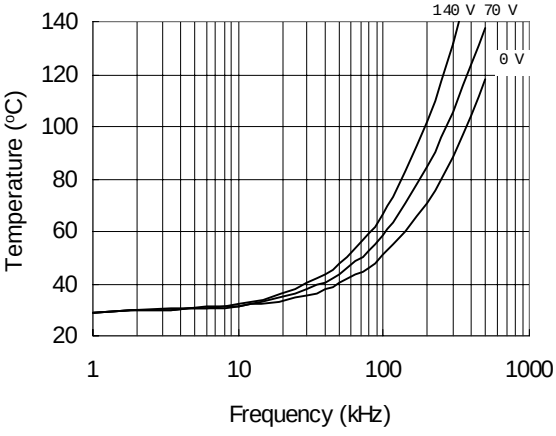


Figure 33. IRS2109 vs Frequency (IRFPE50)
R_{gate} = 10 Ω, V_{CC} = 15 V

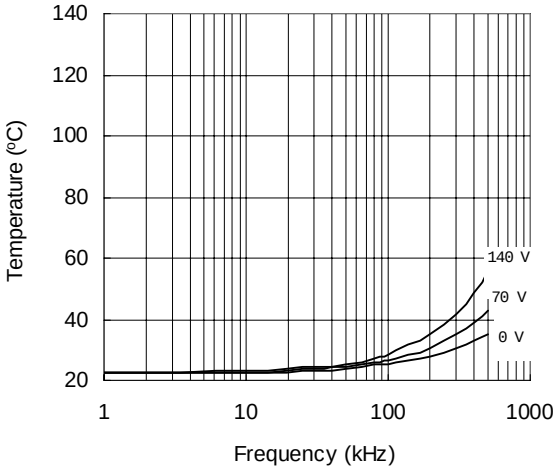


Figure 34. IRS21094 vs. Frequency (IRFBC20), R_{gate}=33 Ω, V_{CC}=15 V

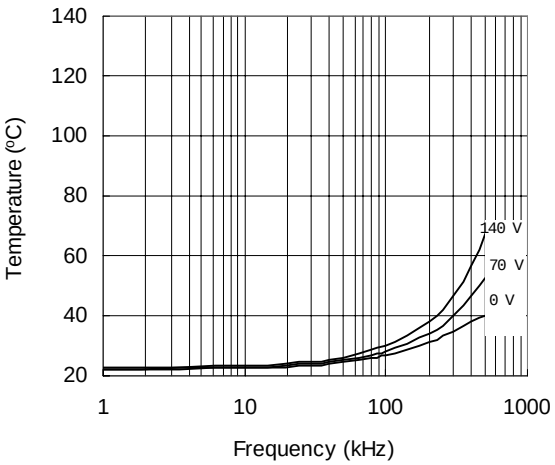


Figure 35. IRS21094 vs. Frequency (IRFBC30), R_{gate}=22 Ω, V_{CC}=15 V

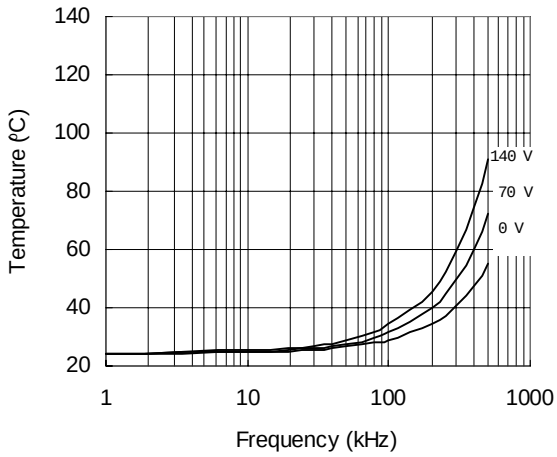


Figure 36. IRS21094 vs. Frequency (IRFBC40), R_{gate}=15 Ω, V_{CC}=15 V

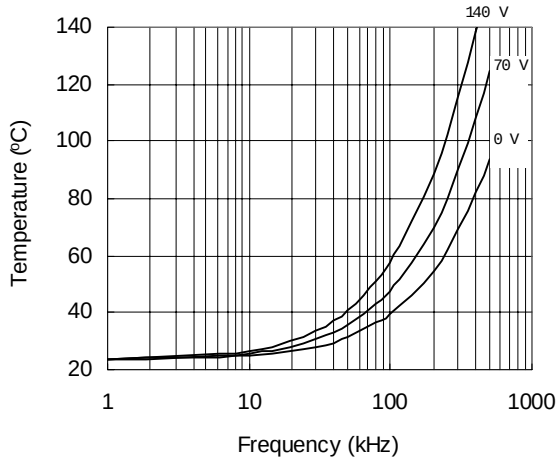


Figure 37. IRS21094 vs. Frequency (IRFPE50), R_{gate}=10 Ω, V_{CC}=15 V

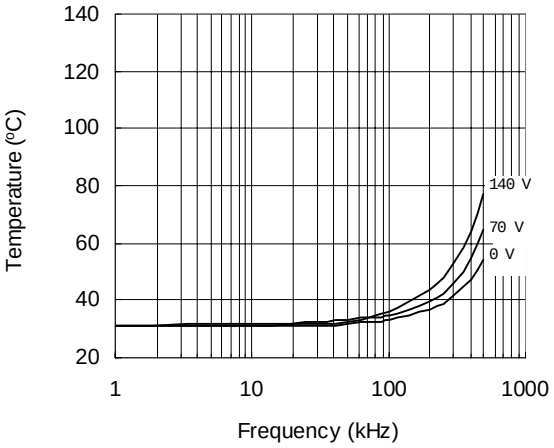


Figure 38. IRS2109S vs. Frequency (IRFBC20), R_{gate}=33 Ω, V_{CC}=15 V

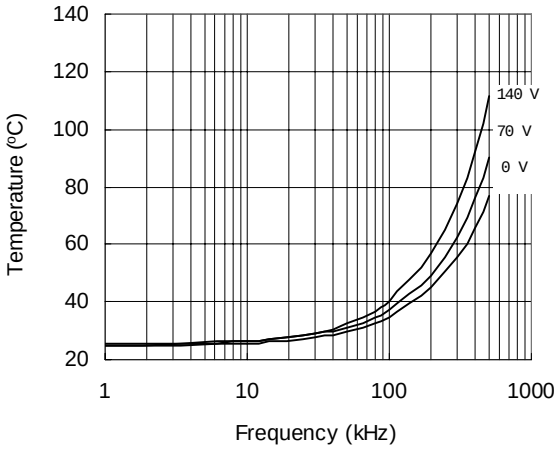


Figure 39. IRS2109S vs. Frequency (IRFBC30), R_{gate}=22 Ω, V_{CC}=15 V

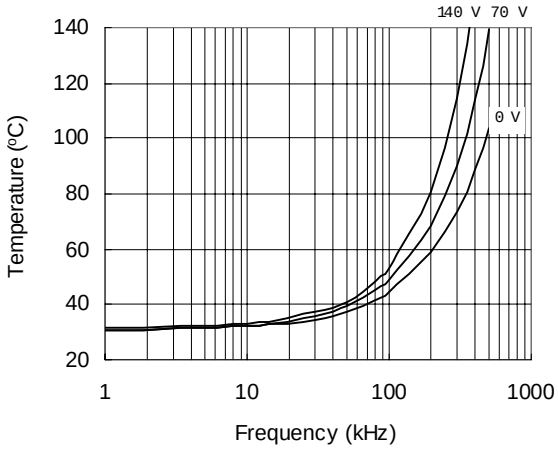


Figure 40. IRS2109S vs. Frequency (IRFBC40), R_{gate}=15 Ω, V_{CC}=15 V

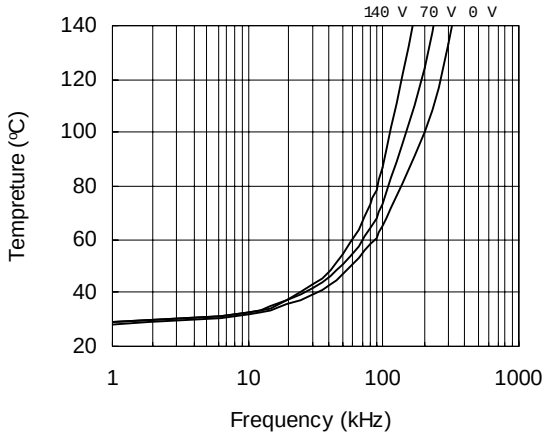


Figure 41. IRS2109S vs. Frequency (IRFPE50), R_{gate}=10 Ω, V_{CC}=15 V

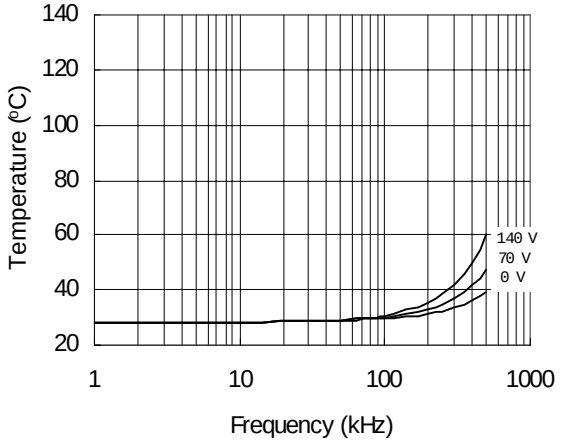


Figure 42. IRS21094S vs. Frequency (IRFBC20), R_{gate}=33 Ω, V_{cc}=15 V

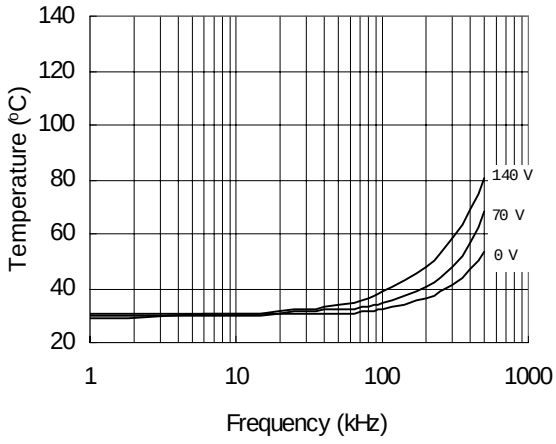


Figure 43. IRS21094S vs. Frequency (IRFBC30), R_{gate}=22 Ω, V_{cc}=15 V

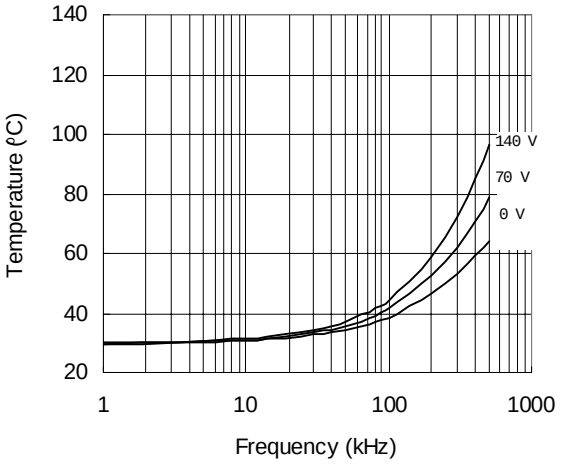


Figure 44. IRS21094S vs. Frequency (IRFBC40), R_{gate}=15 Ω, V_{cc}=15 V

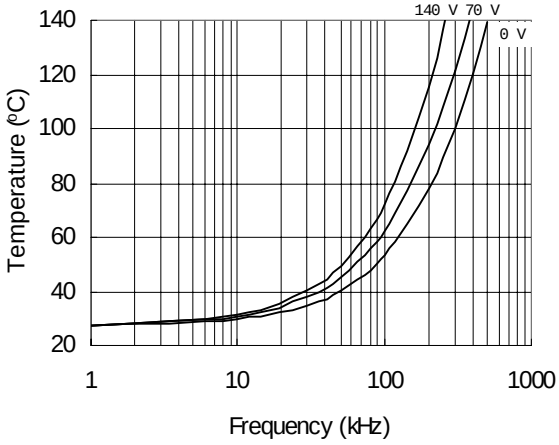
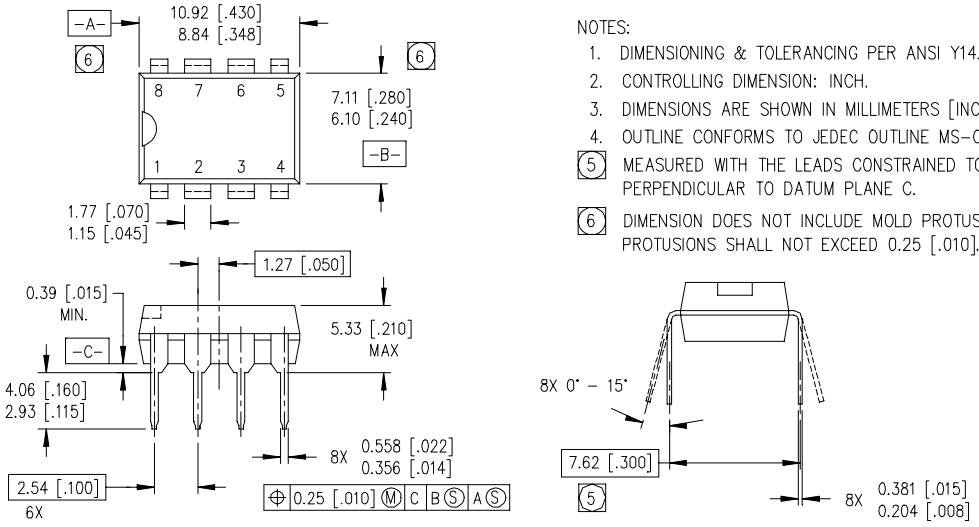


Figure 45. IRS21094S vs. Frequency (IRFPE50), R_{gate}=10 Ω, V_{cc}=15 V

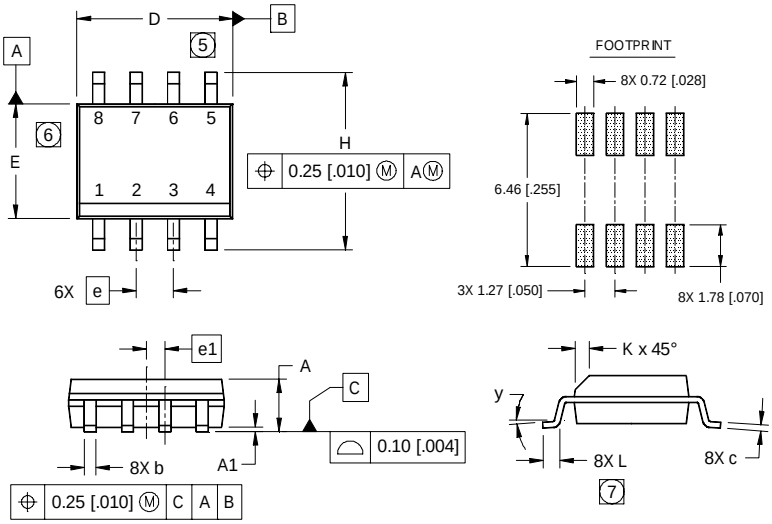
Case Outlines



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

8 Lead PDIP

01-6014
01-3003 01 (MS-001AB)

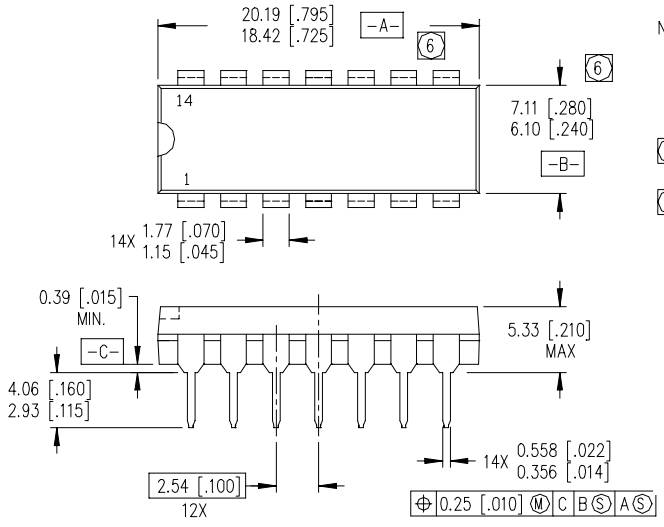


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

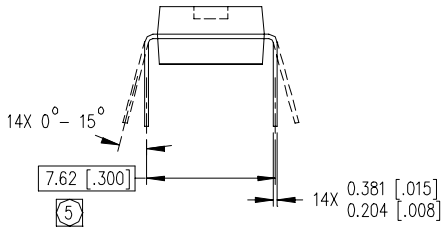
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

01-6027
01-0021 11 (MS-012AA)

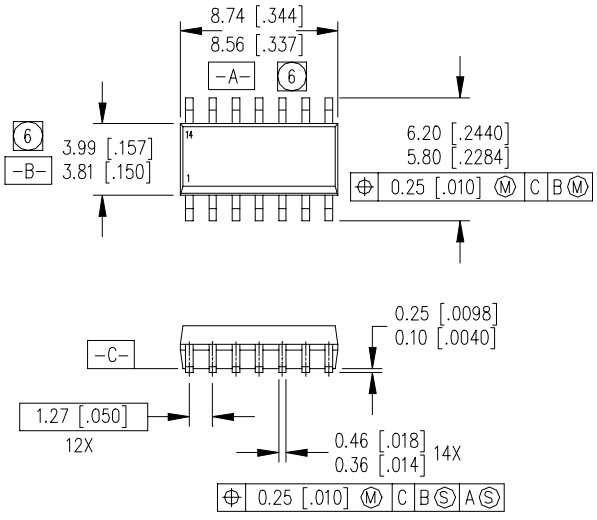


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AC.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

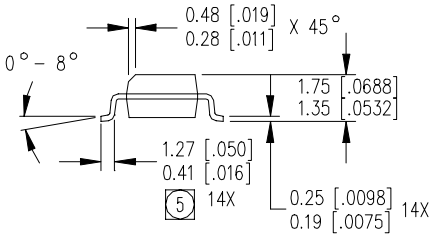


14 Lead PDIP

01-6010
01-3002 03 (MS-001AC)



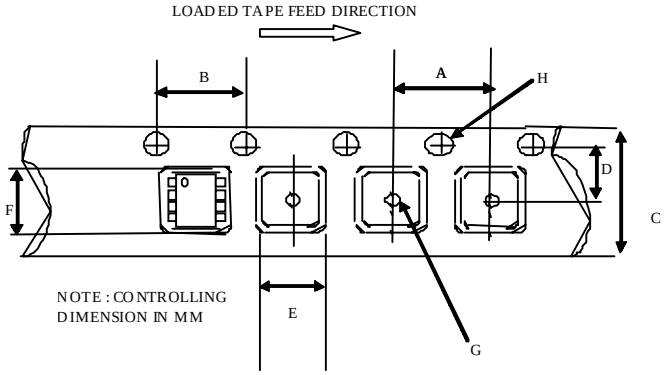
NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2 CONTROLLING DIMENSION: MILLIMETER
3 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4 OUTLINE CONFORMS TO JEDEC OUTLINE MS–012AB.
5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



14 Lead SOIC (narrow body)

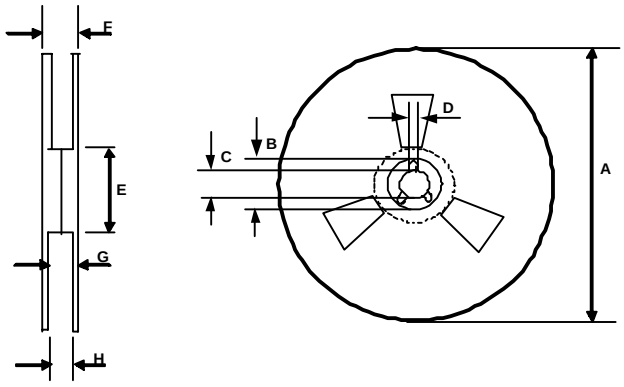
01-6019
01-3063 00 (MS-012AB)

Tape & Reel
8-lead SOIC



CARRIER TAPE DIMENSION FOR 8SOICN

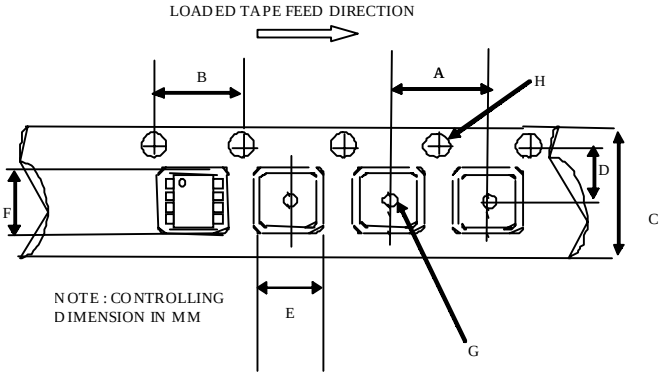
	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

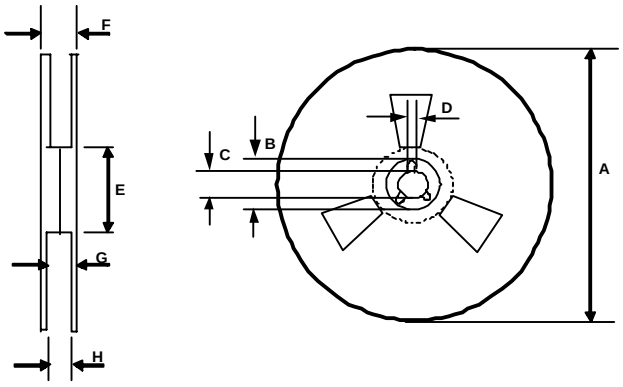
	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Tape & Reel
14-lead SOIC



CARRIER TAPE DIMENSION FOR 14SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	9.40	9.60	0.370	0.378
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 14SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724